

Model Name: GA-Z68XP-UD3R

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
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16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTS X3
18	IT8892 PCI BRIDGE
19	PCI SLOT 1&2
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24	REAR AUDIO JACK
25	VCORE PWM_ISL6364CRZ-1
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SHEET TITLE

28	DISCRETE POWER I
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30	CPU_VTT PWM_ISL6322G
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Gigabyte Technology			
Title			
Cover Sheet			
Size Custom	Document Number GA-Z68XP-UD3R	Rev 1.01	
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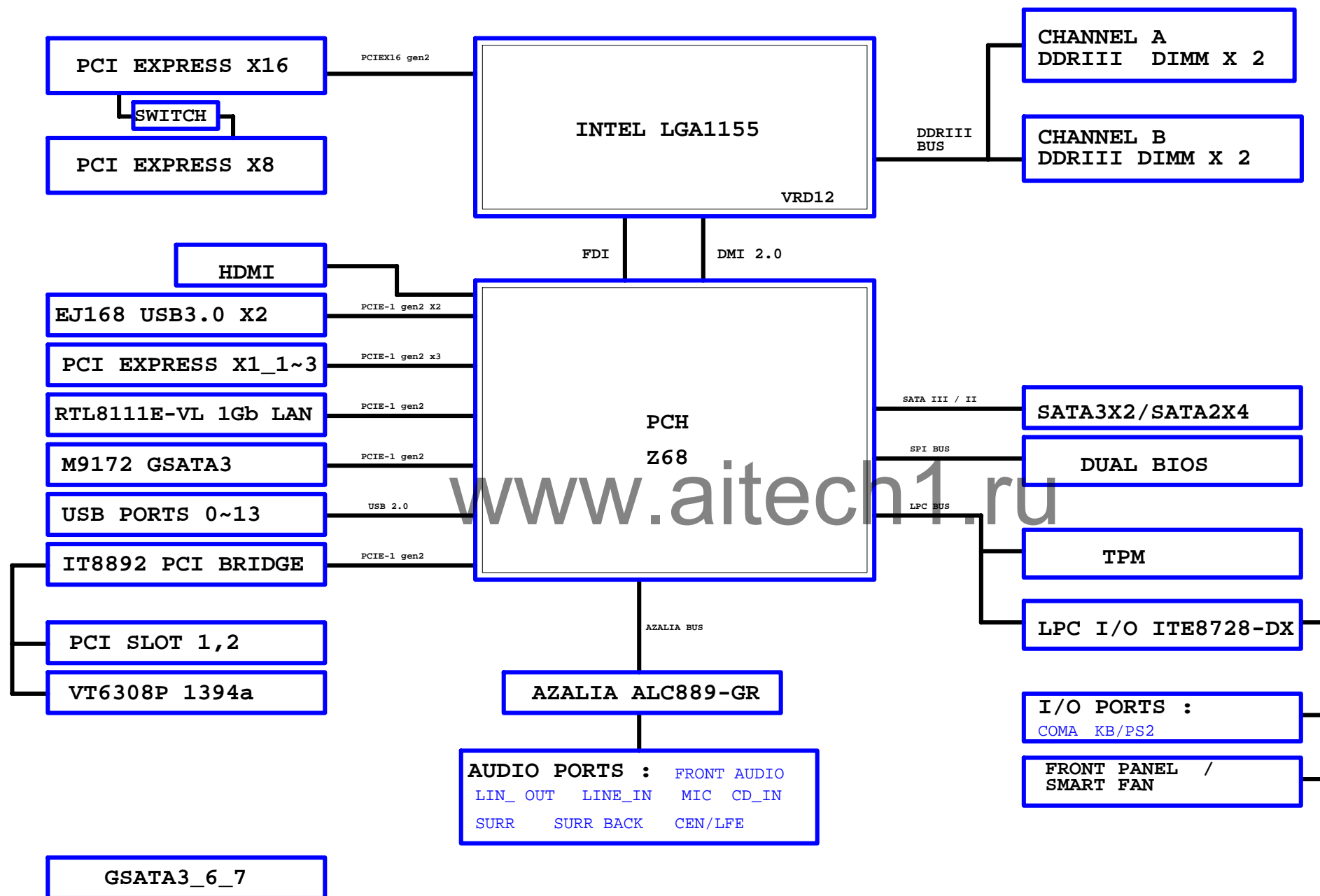
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Component value change history					Circuit or PCB layout change								
Data	Change Item				DATE	Change Item		Reason					
	2011-05-xx					1.0 build ,modify fromP67X-UD3R-B3 1.01							

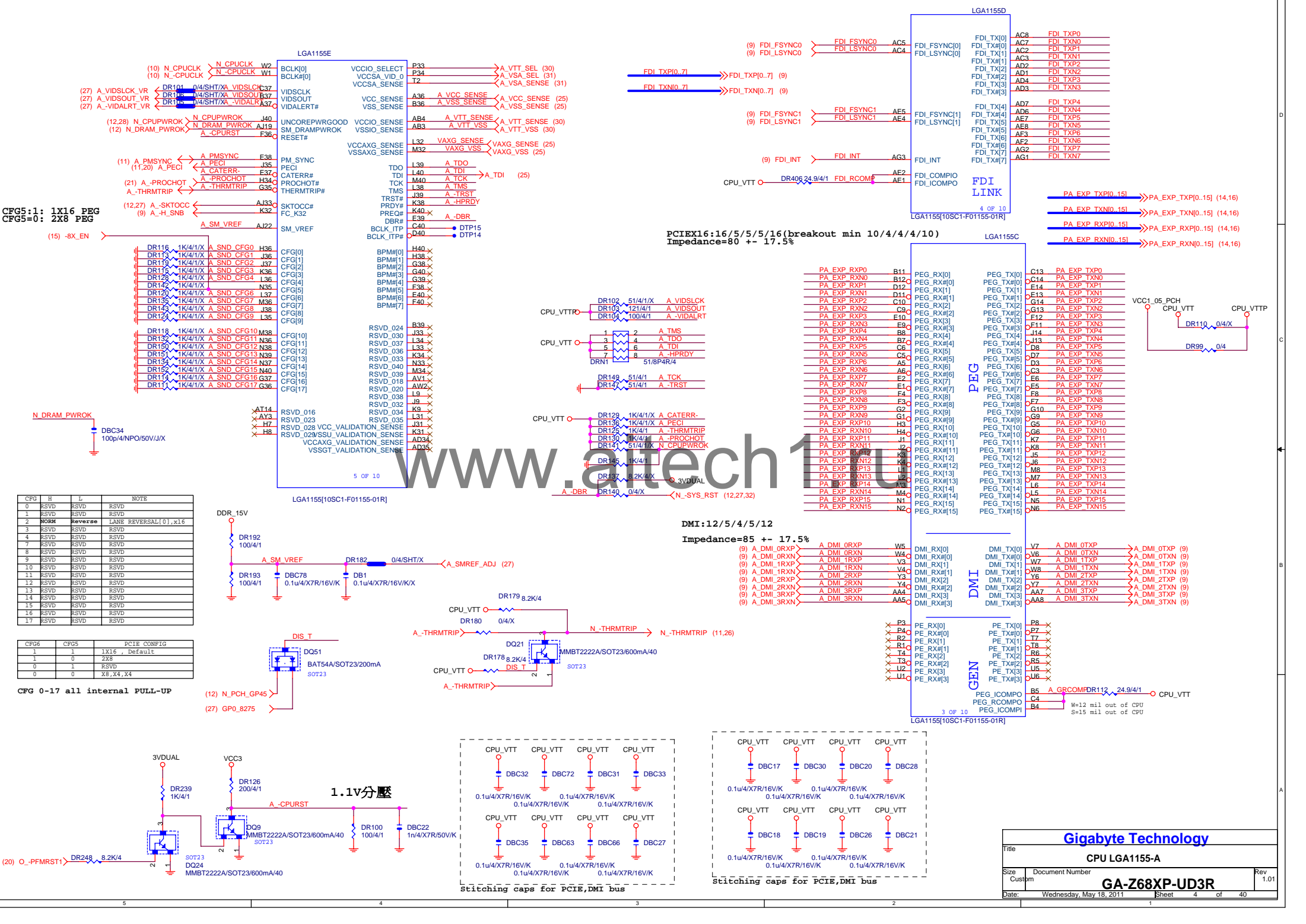
[illegible]

GA-Z68XP-UD3R					Circuit or PCB layout change								
Component value change history					Circuit or PCB layout change								
Data	Change Item				DATE	Change Item		Reason					
	2011-05-xx					1.0 build ,modify fromP67X-UD3R-B3 1.01							

[illegible]

BLOCK DIAGRAM



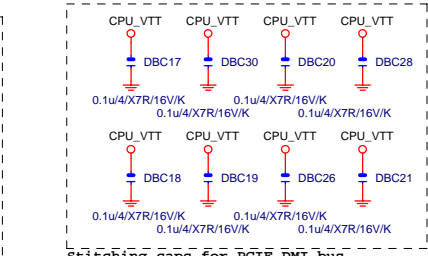
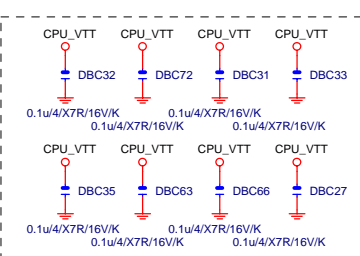
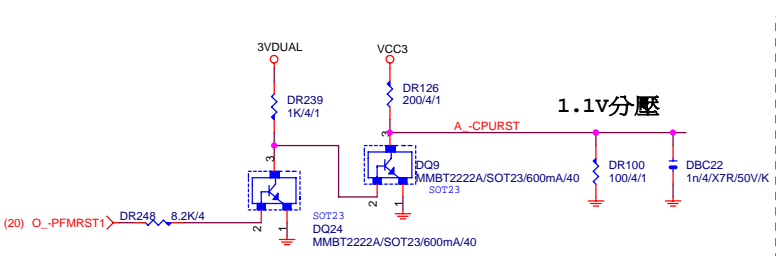


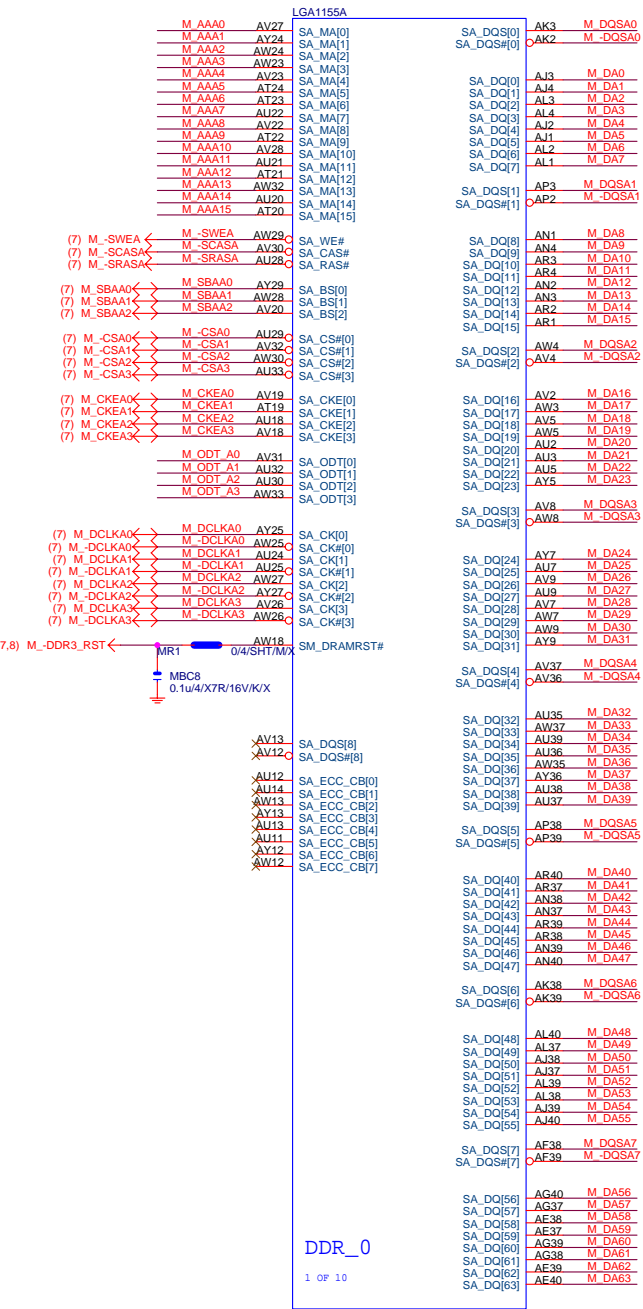
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CFG5:0: 2X8 PEG

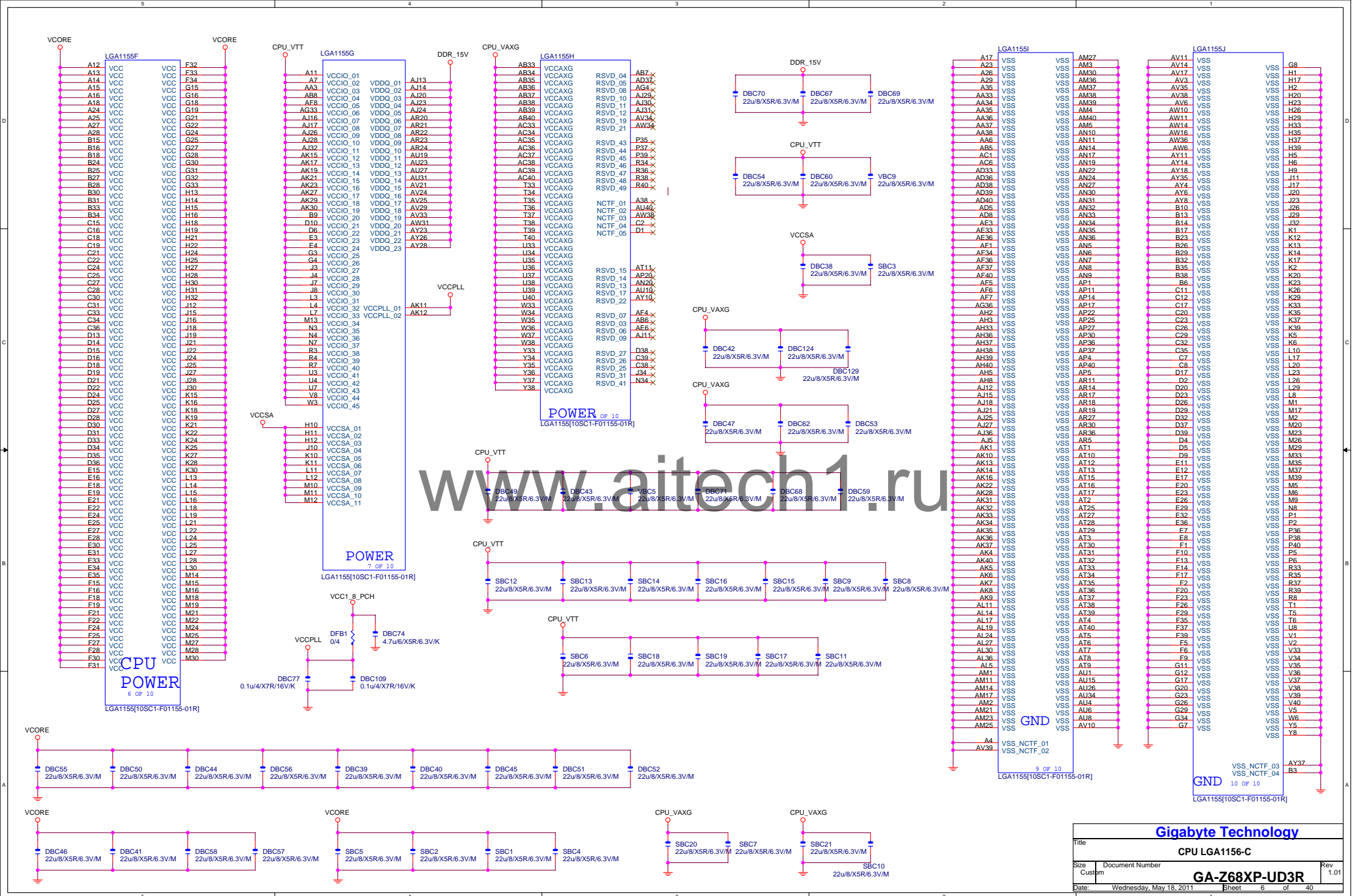
CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	NORM	Reverse	LANE REVERSAL[0]..x16
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1X16, Default
1	0	2X8
0	1	RSVD
0	0	X8_X4_X4

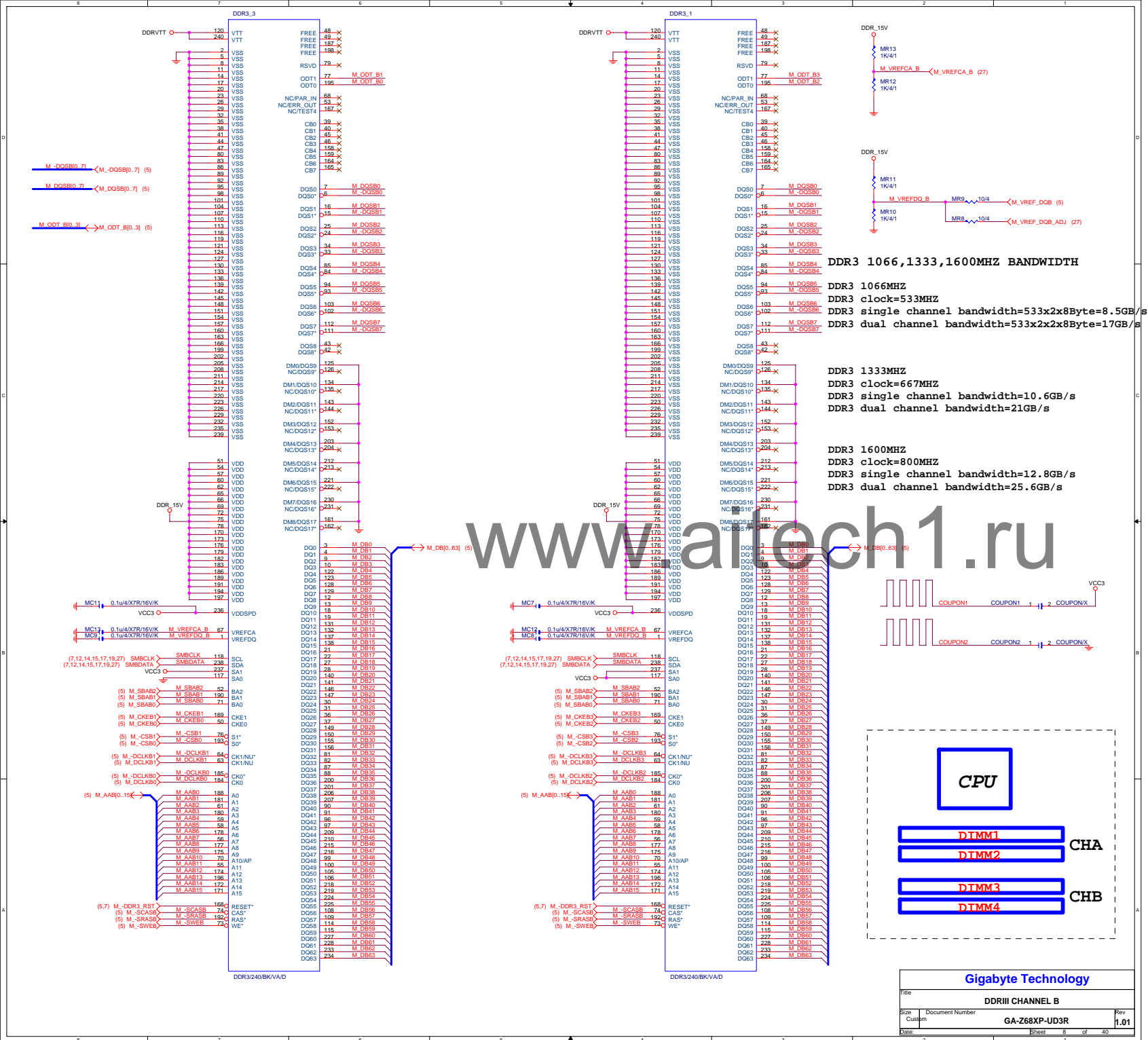
CFG 0-17 all internal PULL-UP

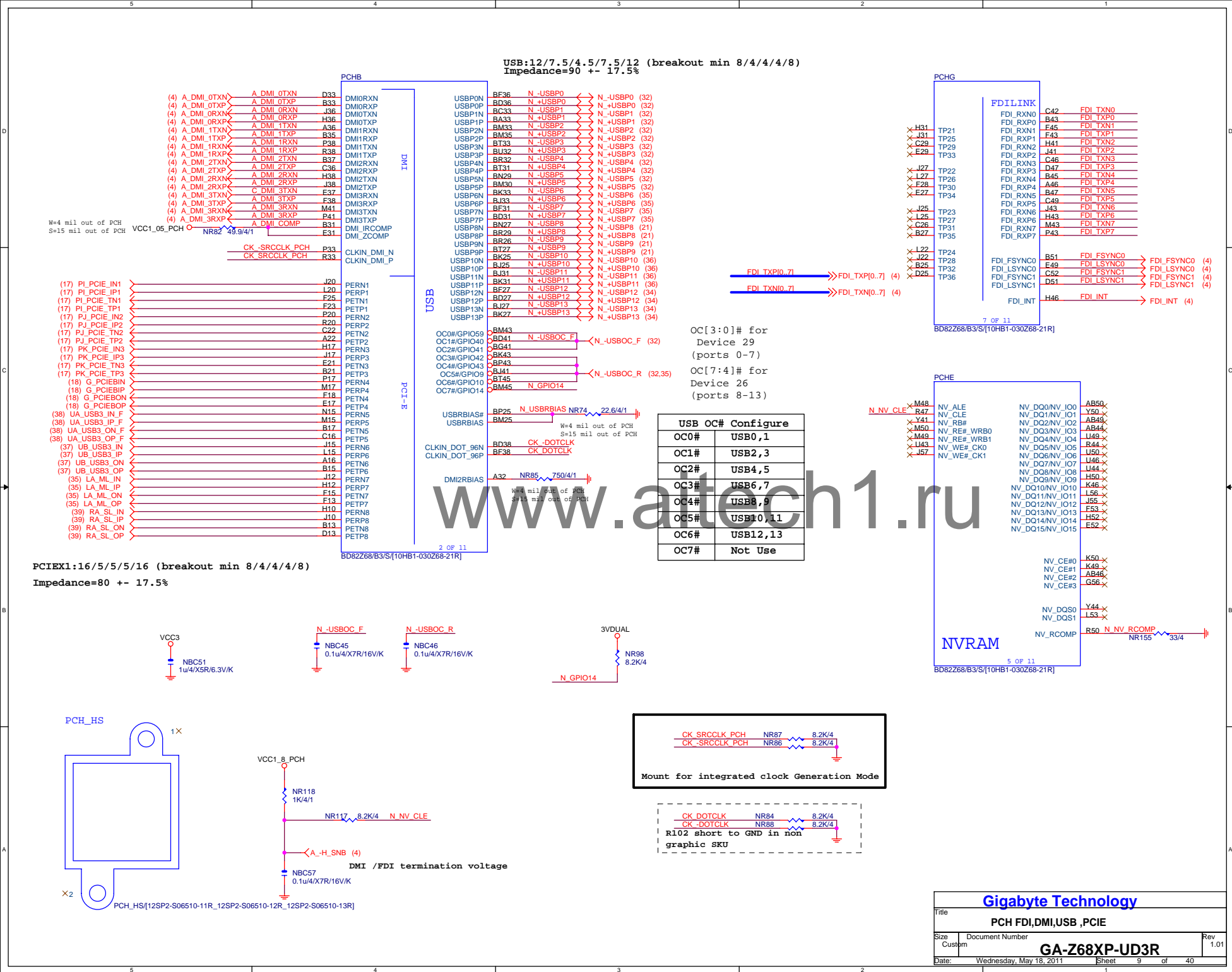


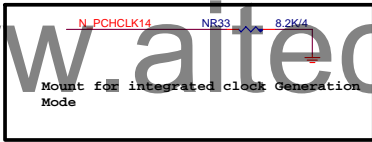
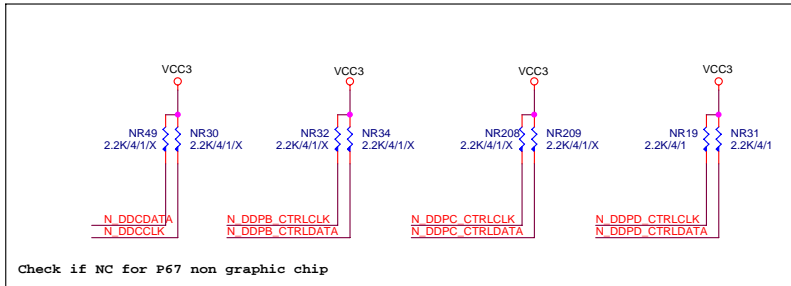
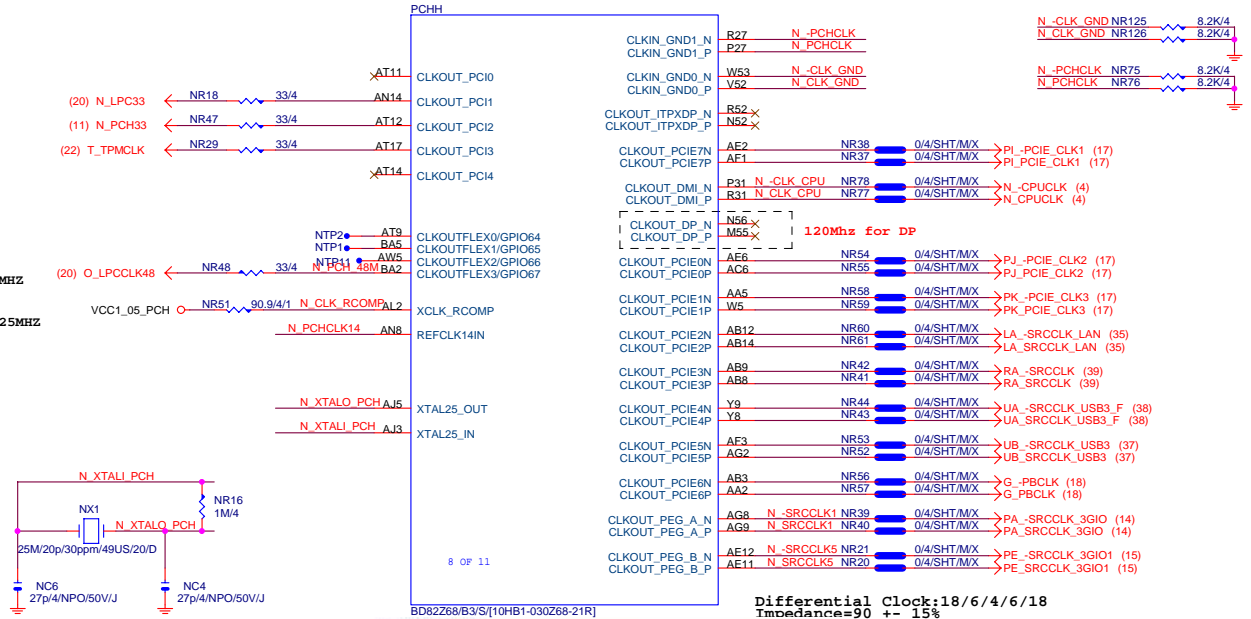
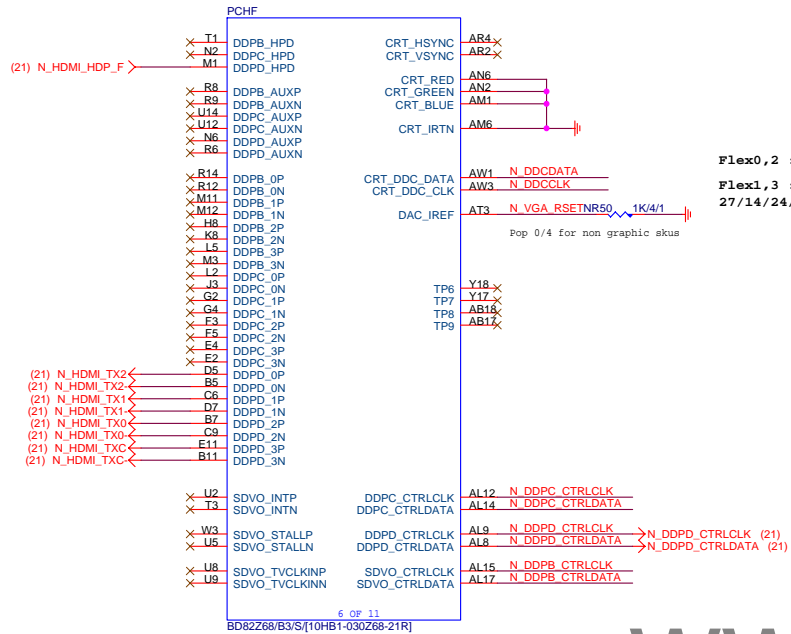












Name	Type	Recommendations	Reason/Impact
SPKR	I/O	Default Mode: Internal weak pull-down. No Reset Mode with TCO Disabled: Connect to Vcc3, 3 with 5.0k-10k Ohm weak pull-up. Do not pull low.	Connect to Vcc3, 3 with 5.0k-10k Ohm weak pull-up. Do not pull low.
SPKTRIP	I/O	Default Mode: Internal pull-up. Trip Block Trip Mode: Connect to ground with 4.7k Ohm weak pull-down resistor.	Connect to ground with 4.7k Ohm weak pull-down resistor.
SATA1GP/SPS019, GNT1#	I/O	Default (NFI) Link turn SATA1GP/SPS019 and GNT1# floating. No pull-up required. Reset from PCI Connect SATA1GP/SPS019 to ground with 1k Ohm pull-down resistor. Leave GNT1# floating. Reset from LPC Connect both SATA1GP/SPS019 and GNT1# to ground with 1k Ohm pull-down resistor.	If LFC is selected BIOS may still be placed on LFC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid decoder in order to boot. Resetting to PCI is intended for debug/testing only. Boot BIOS Configuration (direct to LPC/PCI) by functional strap or via Boot BIOS Destination bit will not affect SPI accesses initiated by Management Engine or Integrated BMC LAM.
SATA2P/SPS020	I/O	Do not pull low.	BIOS strap for server platform ONLY
HDA_SDD	I/O	Default Do not pull high.	Flash Descriptor Override
Disable HE in Manufacturing Mode	I/O	Connect to Vcc3/GND4 with 1k Ohm pull-up resistor through a jumper.	Flash Descriptor Override
SPI_M0N0	I/O	Internal weak pull down. Do not pull high.	EMI R.F. Termination Voltage
SP_TVS	I/O	Internal weak pull up. Do not pull low.	EMI Termination Voltage
HDA_STM0	I/O	Internal weak pull down. Do not pull up.	On die Pk, Vb voltage selector
SPS015	I/O	Enable T1S: Pull up with 1k Ohm to Vcc3/GND3.3. Default (Disable T1S): Leave NC. Internal pull down.	Tx3 confidentiality
SPS08	I/O	RTN Leave floating. Do not pull low. FECN Pull low with 1k Ohm to ground.	PCIE Can be override by softstrap through RTN.
SPS02R	I/O	Internal weak pull up. Do not pull low.	On die Pk, voltage regulator
SATA3GP/SPS036	I/O	Internal weak pull down. Do not pull high.	
SATA3GP/SPS037	I/O	Internal weak pull down. Do not pull high.	

Gigabyte Technology		
Title PCH DISPLAY ,CLK BUFFER		
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SATA:20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

PCHC

PCHA

MB-ID

For WIFI

CL_CLK1

CL_DATA1#

CL_RST1#

CLINK

SATA3

SATA2

FAN

SST

GPIO

HOST

CLINK_SATA_N

CLINK_SATA_P

SATALED#

SATAICOMPI

SATAICOMPO

SATA0GP/GPIO21

SATA1GP/GPIO19

SATA2GP/GPIO36

SATA3GP/GPIO37

SATA4GP/GPIO16

SATA5GP/GPIO49

SATA3COMPI

SATA3RCOMPO

SATA3BIAS

A20GATE

INIT3_3V#

RCIN#

SERIRQ

THRMTRIP#

PECI

PMSYNCH

TP16

NR177

NR178

NR179

NR180

NR181

NR182

NR183

NR184

NR185

NR186

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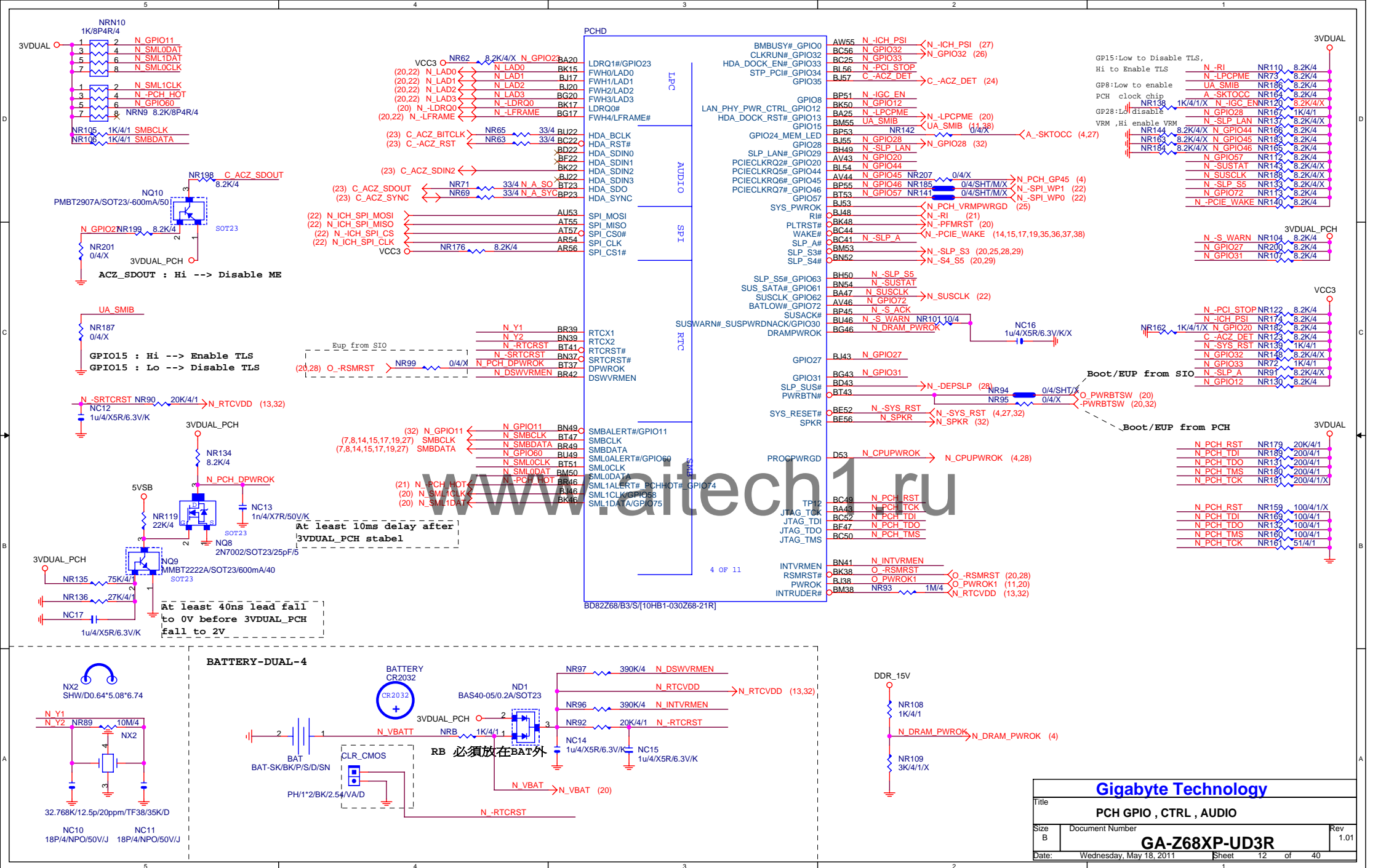
NR456

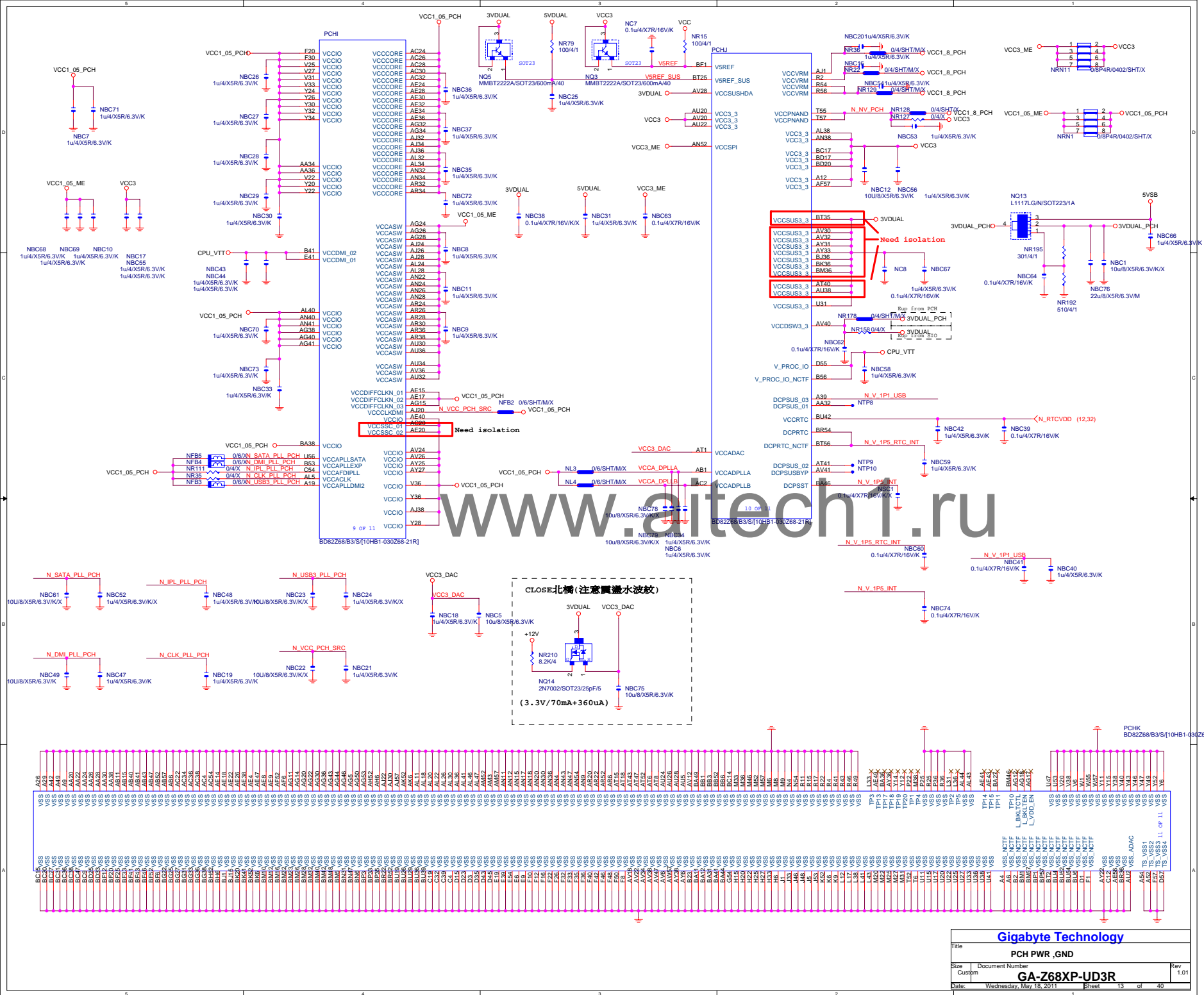
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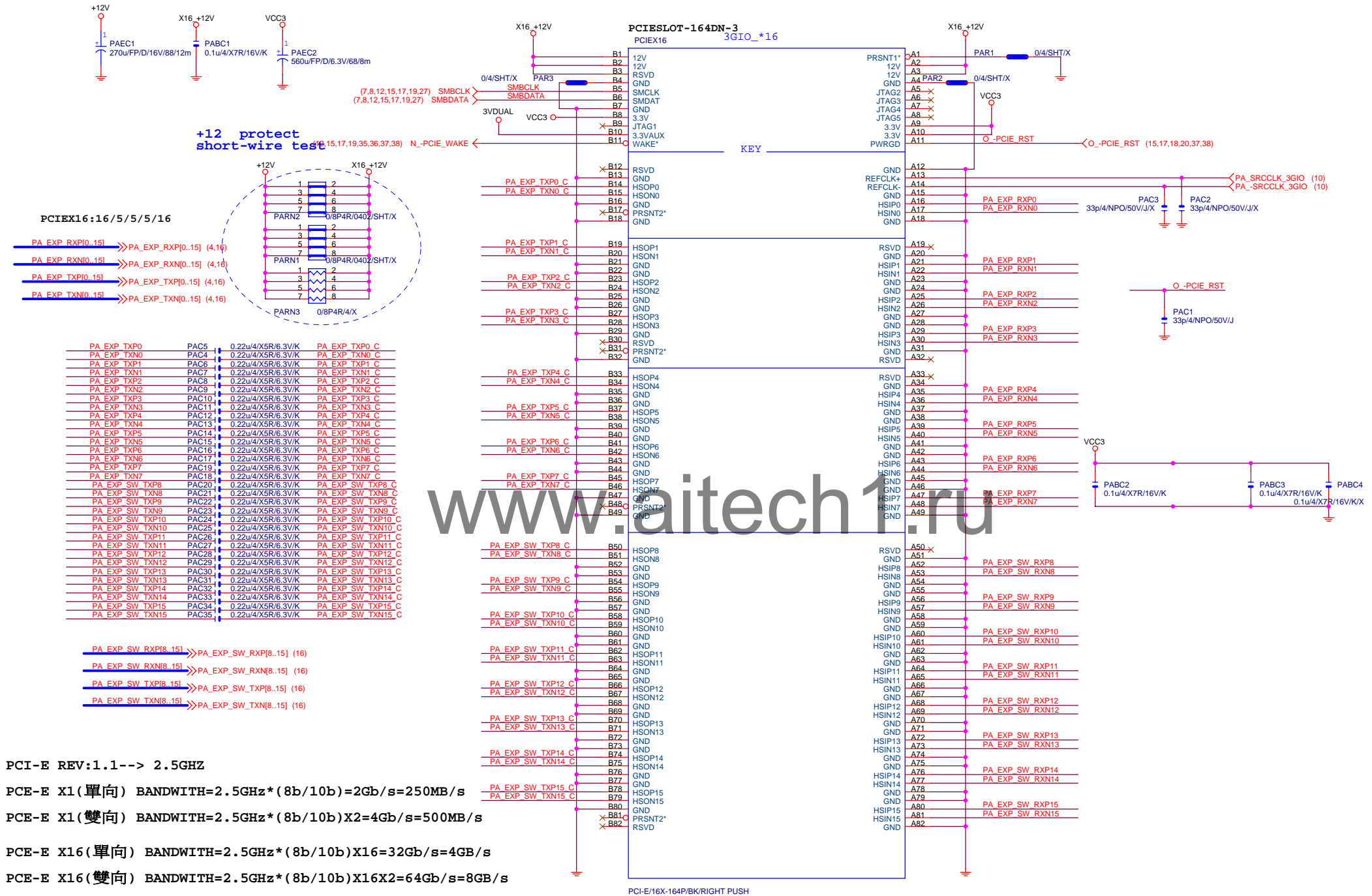
NR458

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NR460

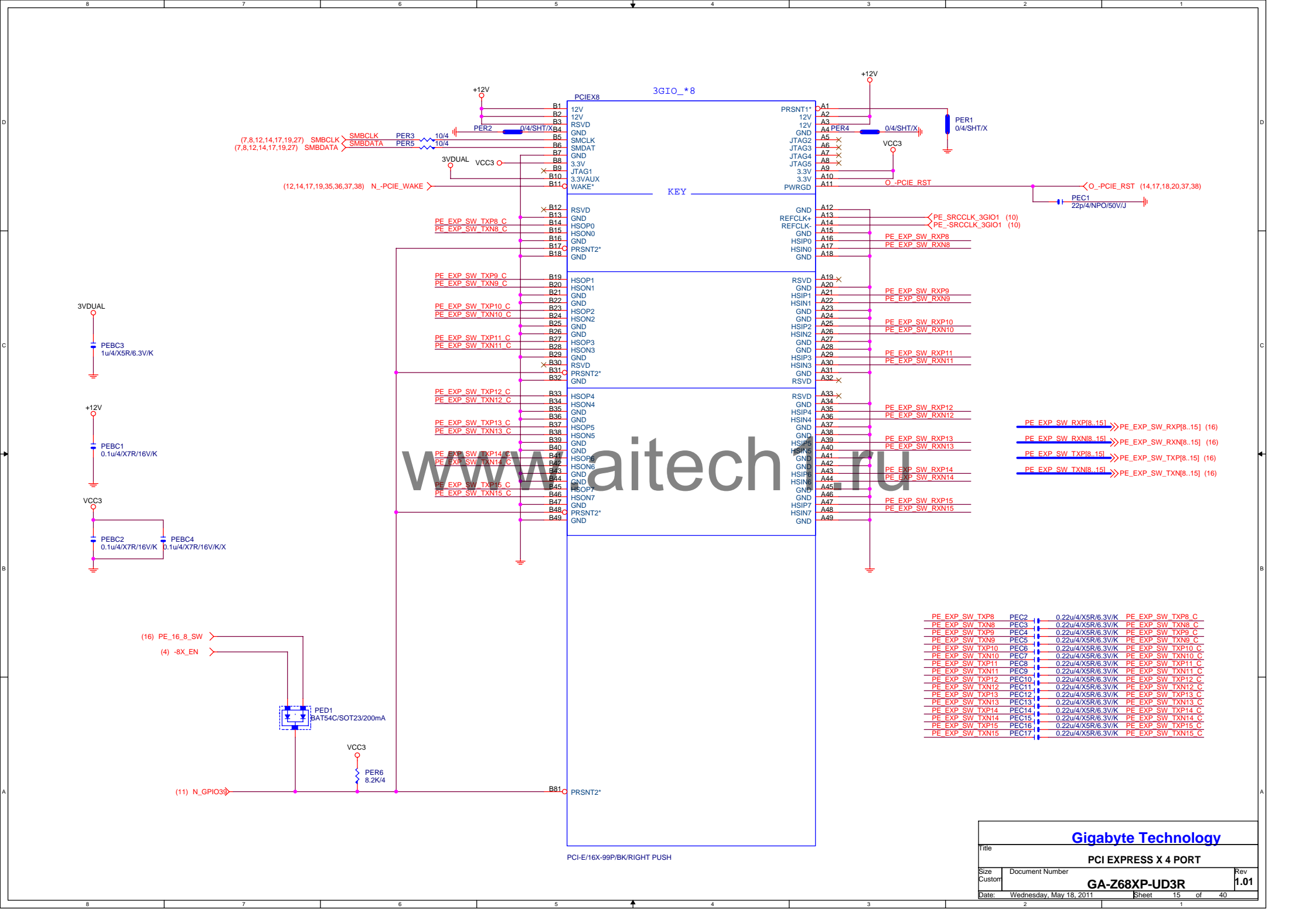


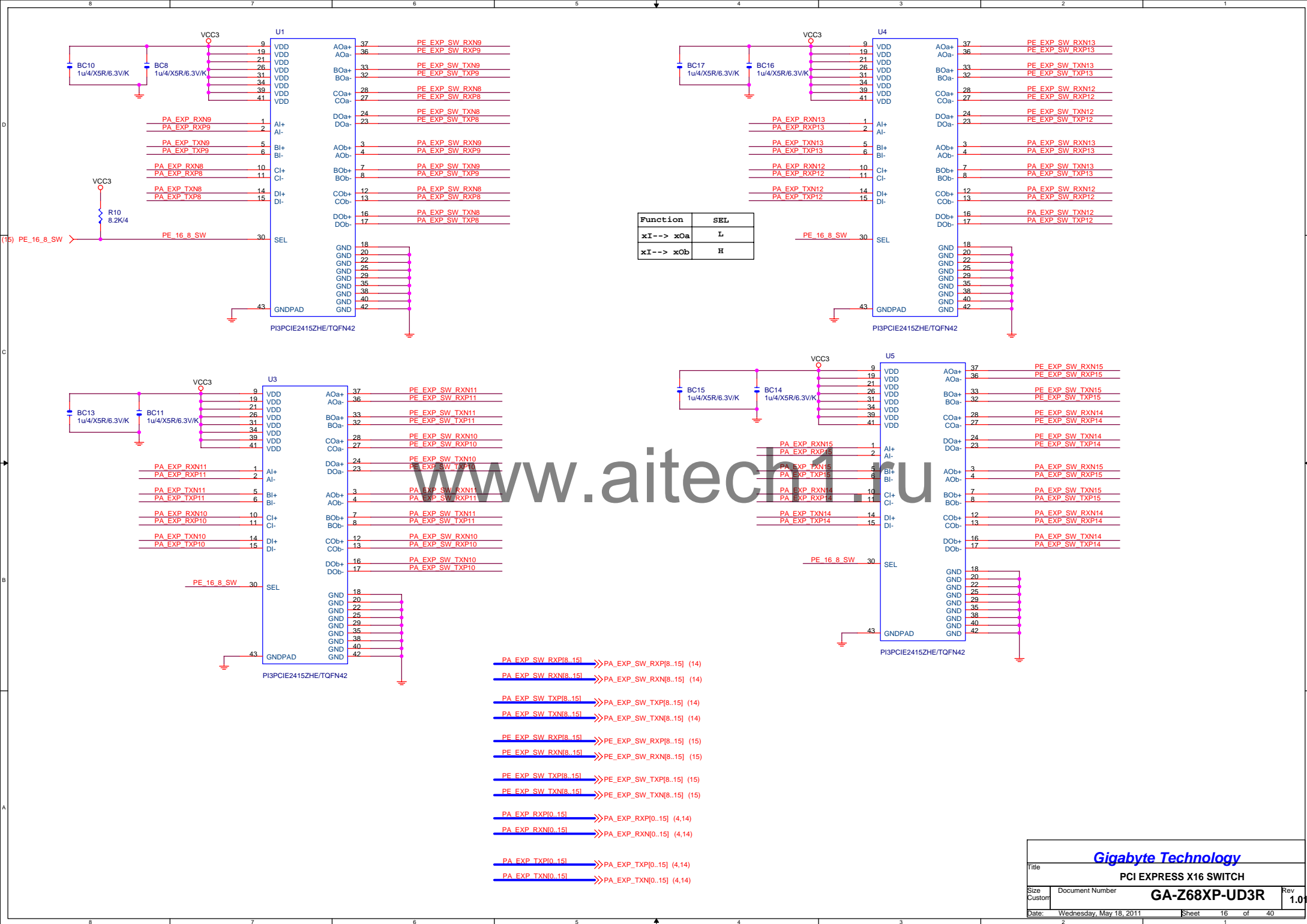


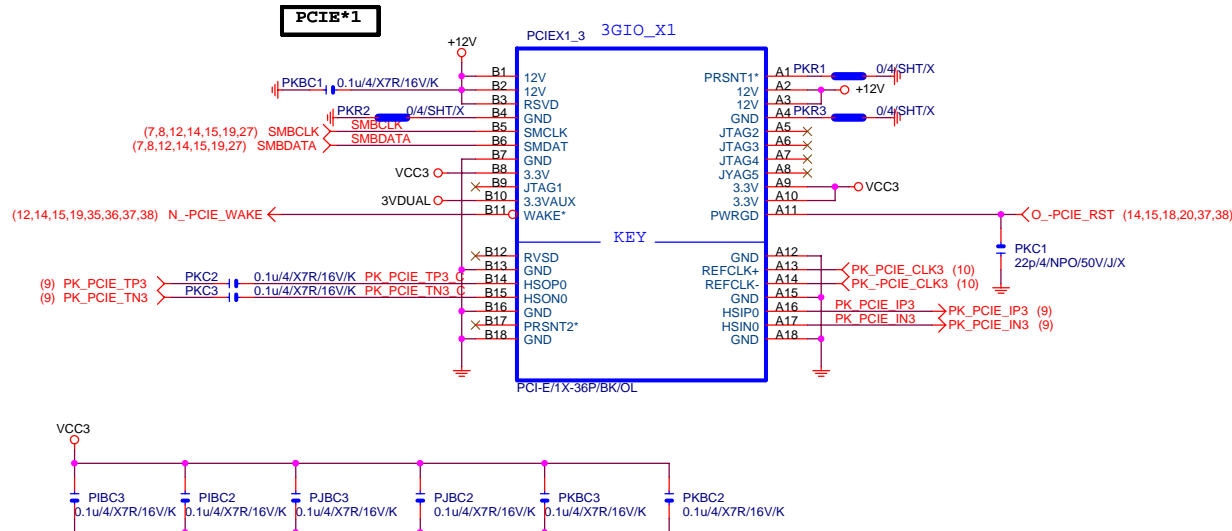
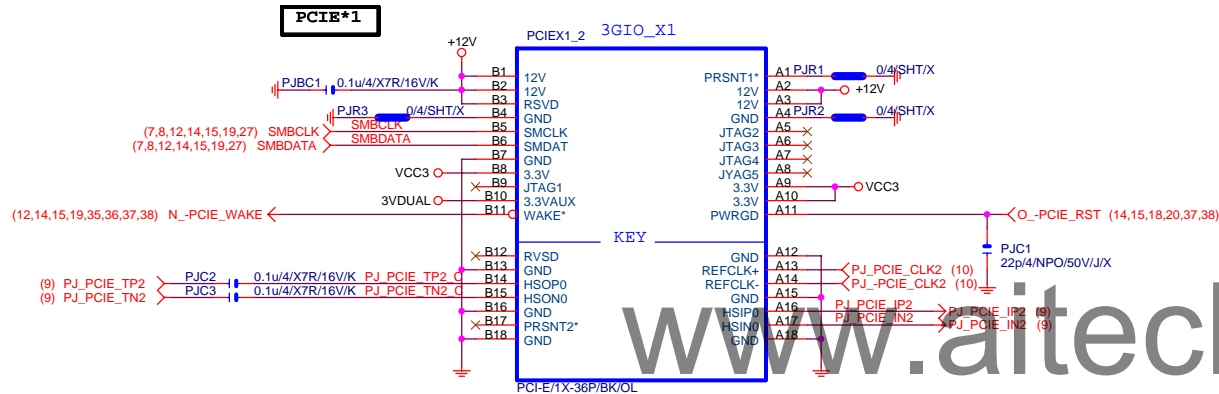
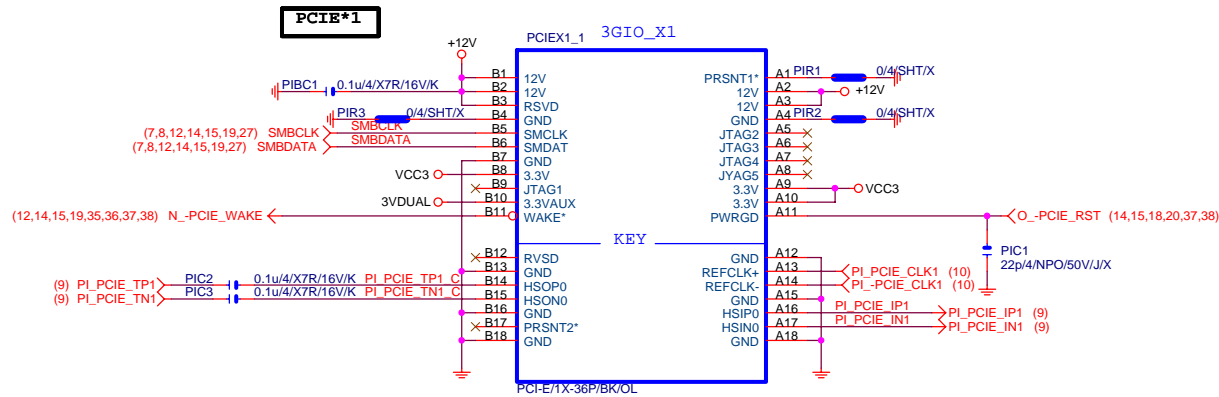


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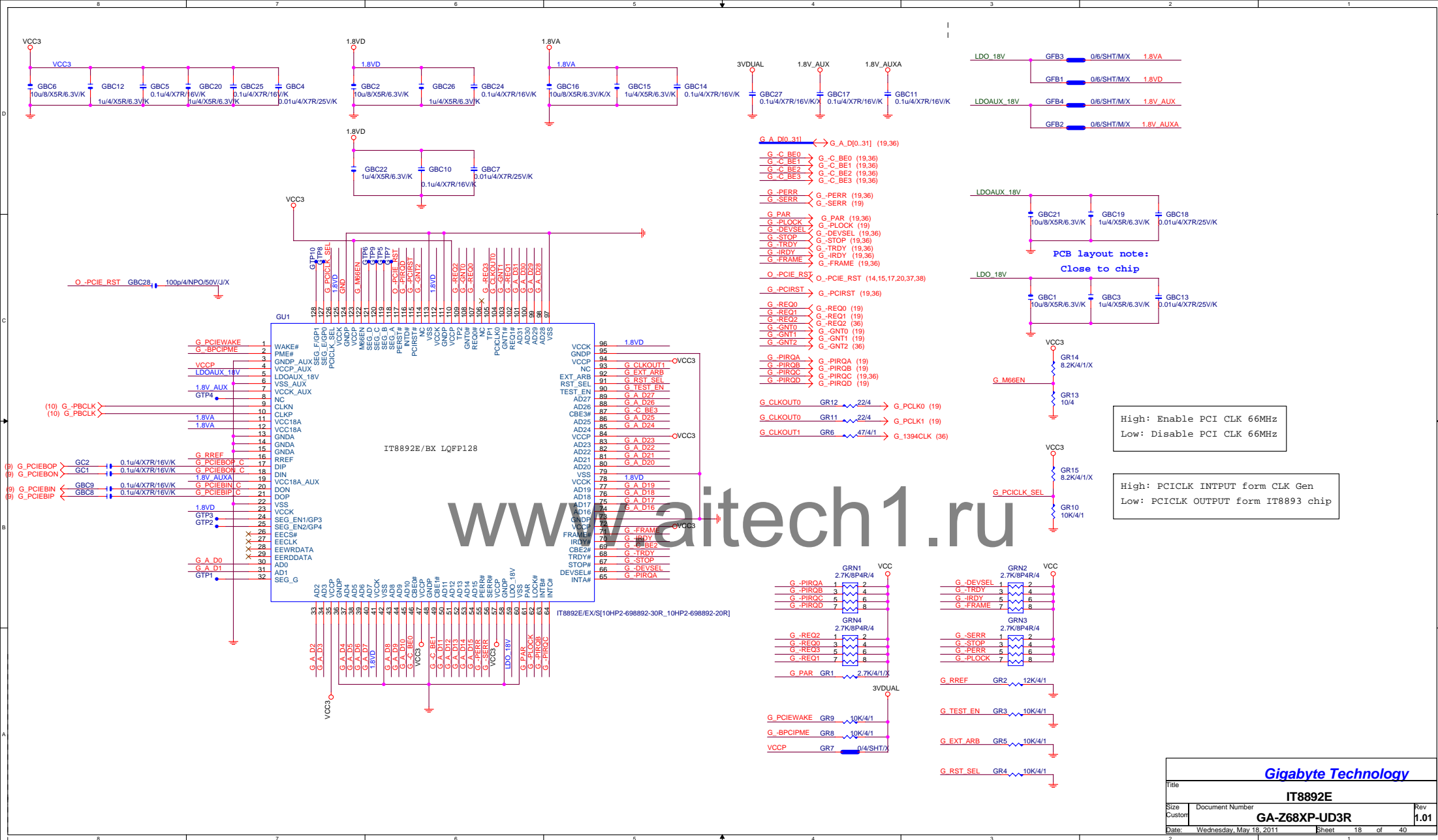


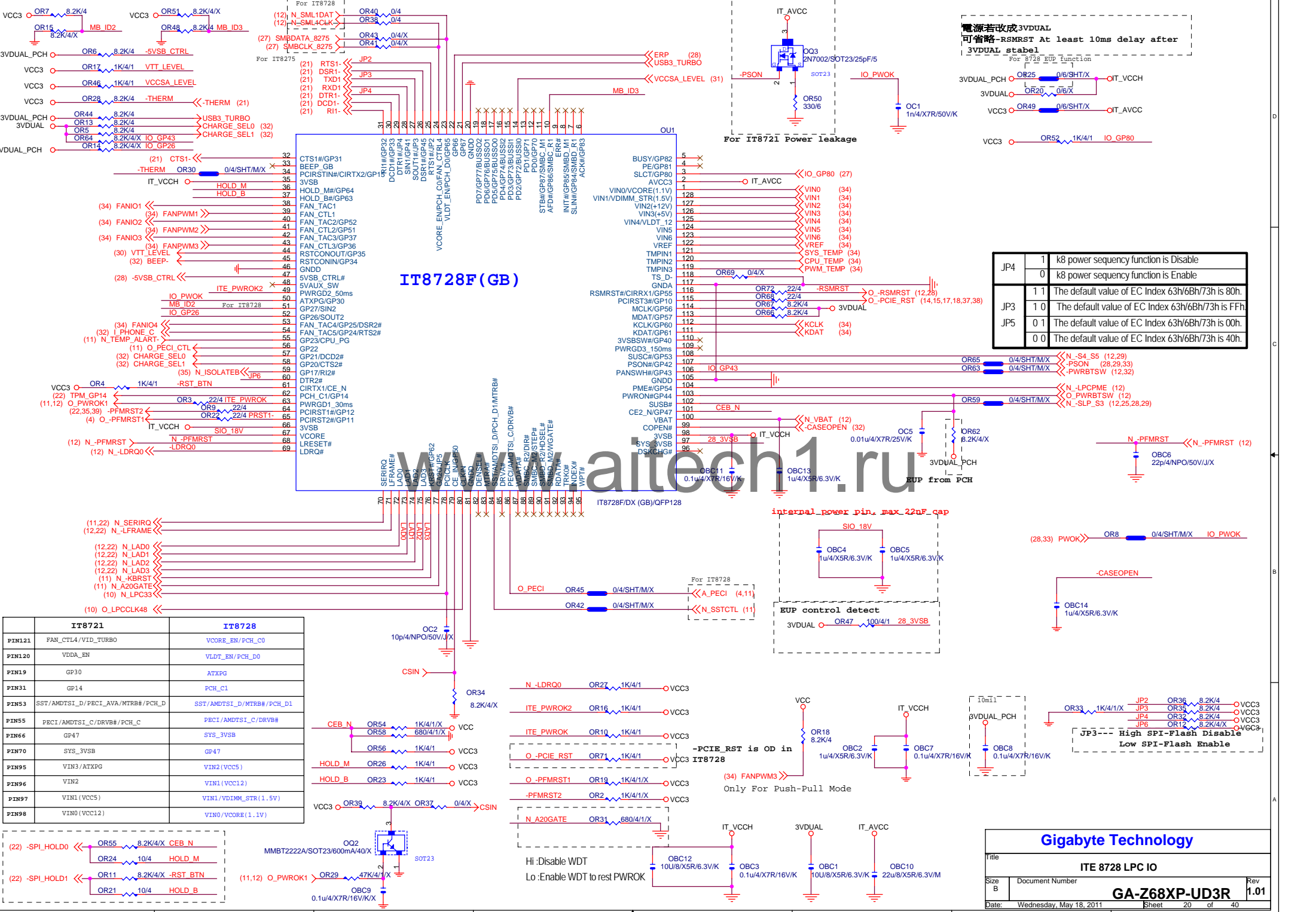




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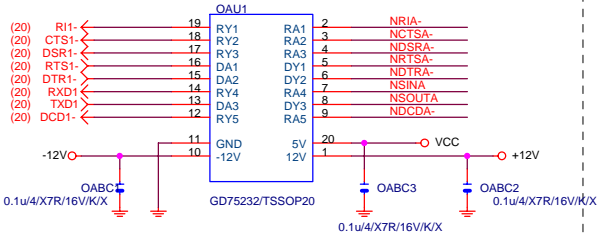
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Size	Document Number	Rev	
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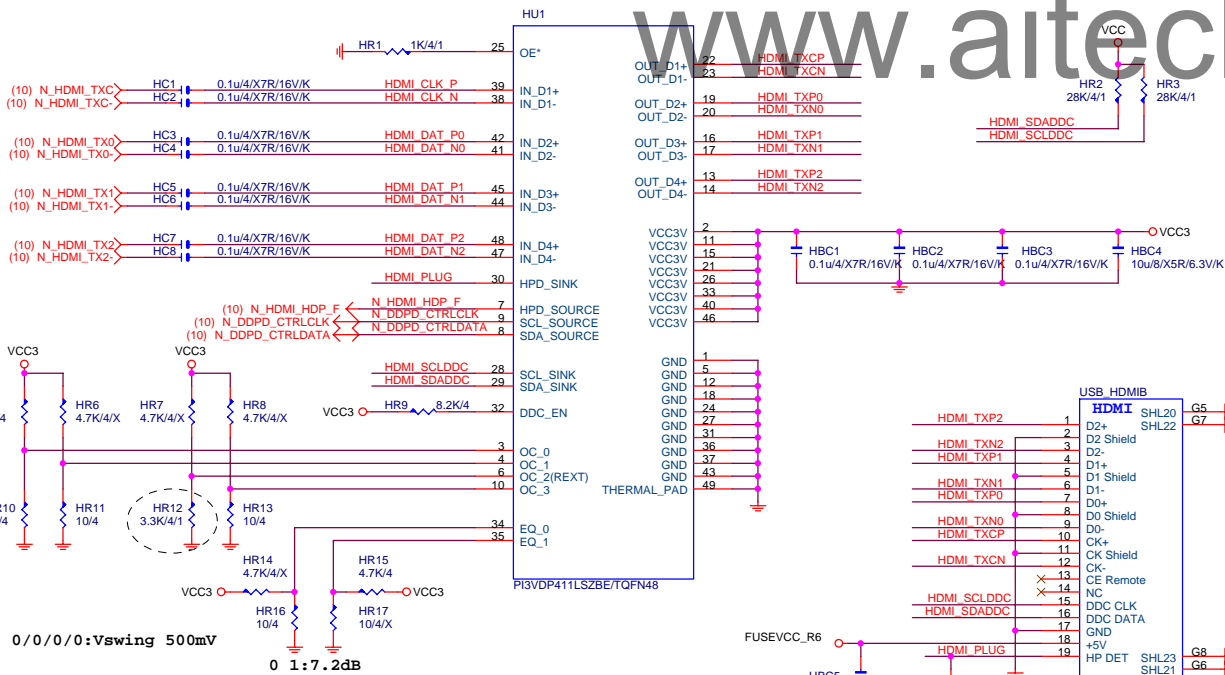
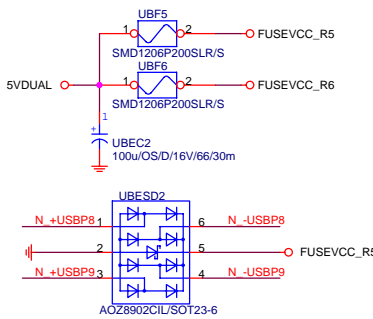
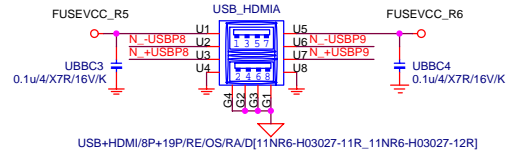
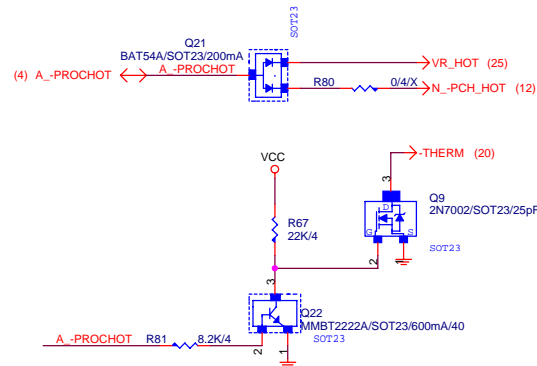
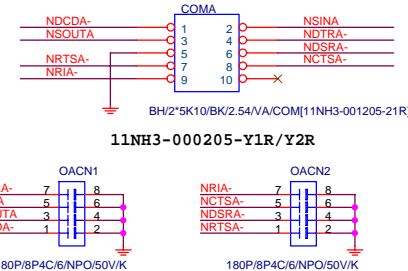
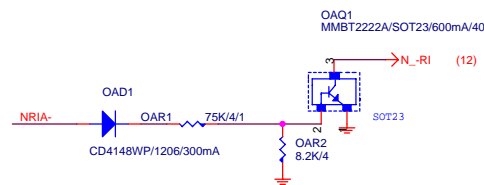


	IT8721	IT8728
PIN121	FAN_CTL4/VID_TURBO	VCORE_EN/PCH_C0
PIN120	VDDA_EN	VLDOT_EN/PCH_D0
PIN19	GP30	ATXPG
PIN31	GP14	PCH_C1
PIN53	SST/AMDTSI_D/PCI_AVA/MTRB#/PCH_D	SST/AMDTSI_D/MTRB#/PCH_D1
PIN55	PECI/AMDTSI_C/DRVB#/PCH_C	PECI/AMDTSI_C/DRVB#
PIN66	GP47	SYS_3VSB
PIN70	SYS_3VSB	GP47
PIN95	VIN3/ATXPG	VIN2 (VCC5)
PIN96	VIN2	VIN1 (VCC12)
PIN97	VIN1 (VCC5)	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0 (VCC12)	VIN0/VCORE(1.1V)

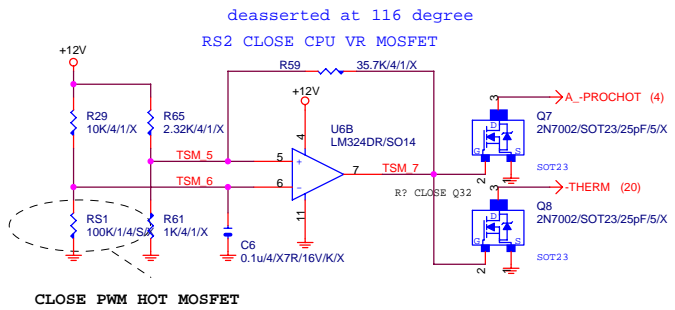
COMA



COM RI



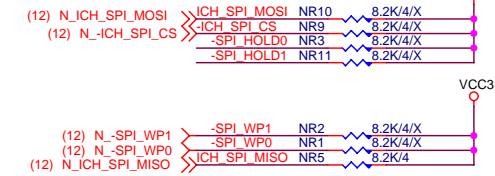
PROHOT



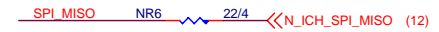
Gigabyte Technology

Title			COM , PROHOT , RUSB ,HDMI
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MOSI For DMI RX Termination Voltage



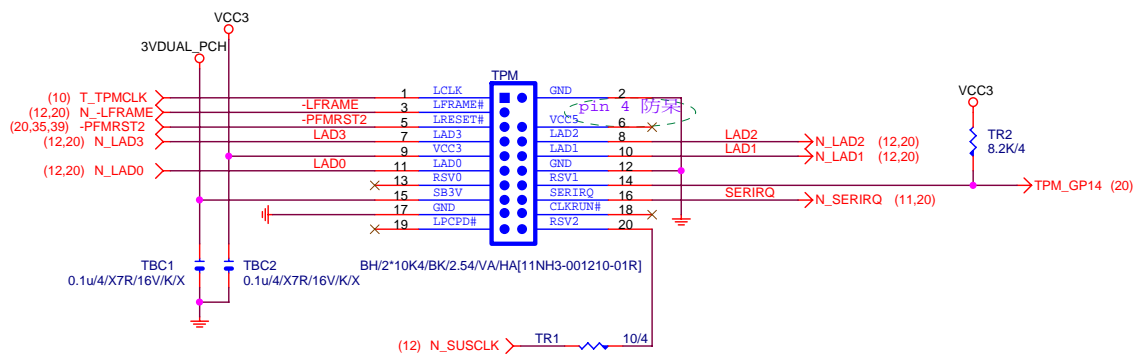
Default int pull up



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

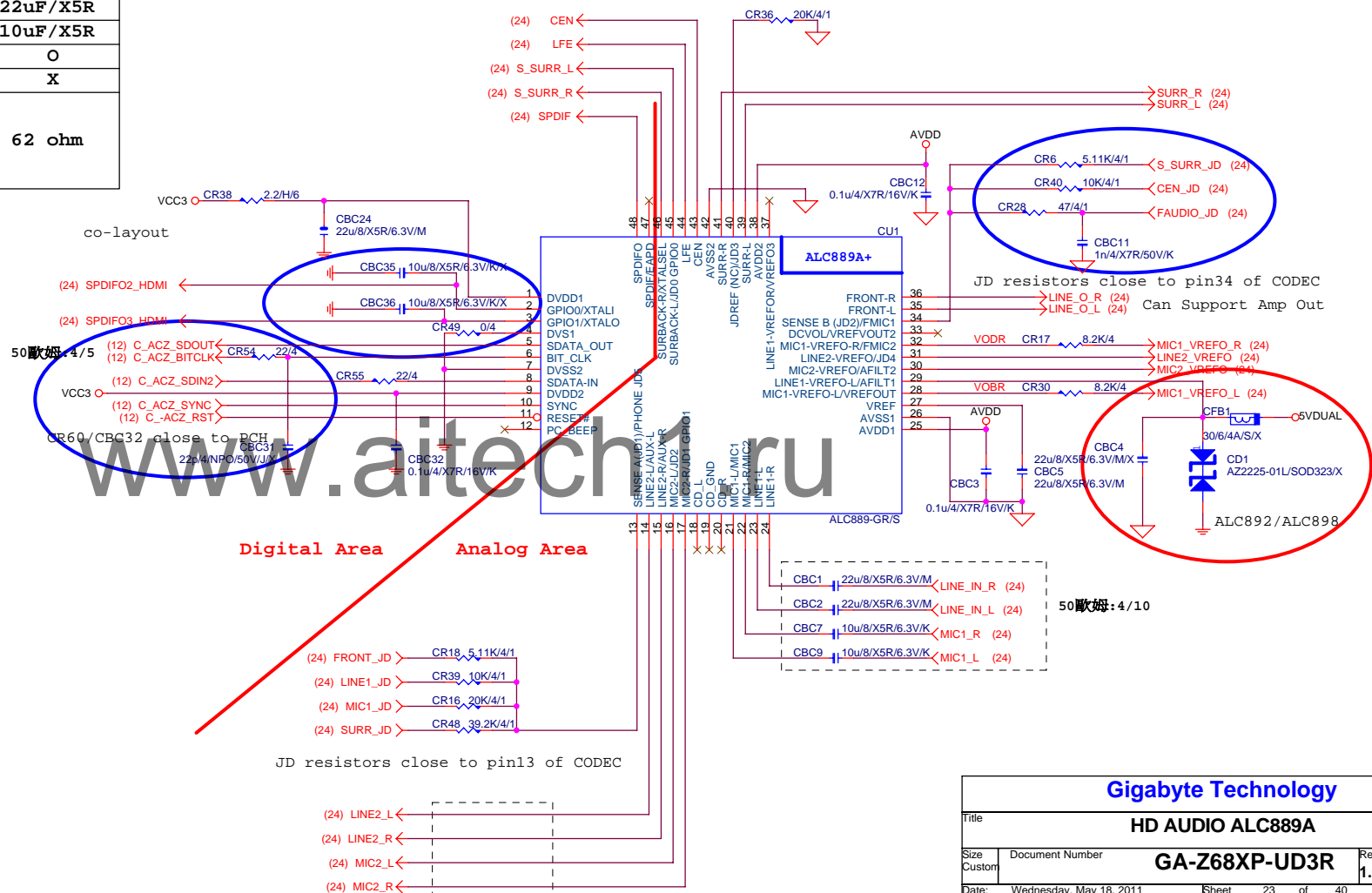
1 means floating
0 means PD 1K

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Gigabyte Technology			
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	ALC889	ALC889B	ALC898/ALC892
CR49	O	O	X
CBC36	X	X	10uF/X5R
CBC35	X	10uF/X5R	X
CR52	O	X	O
CR53	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC7/CBC9/CBC20/CBC15	10uF/X5R	10uF/X5R	10uF/X5R
CFB1/CD1/CBC4	X	X	O
CD2/CD3/CQ3/CQ4	O	O	X
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47/ CR2/CR11/CR14/CR24	62 ohm	62 ohm	62 ohm



Gigabyte Technology

HD AUDIO ALC889A

Title

Document Number

GA-Z68XP-UD3R

Rev

1.01

Date:

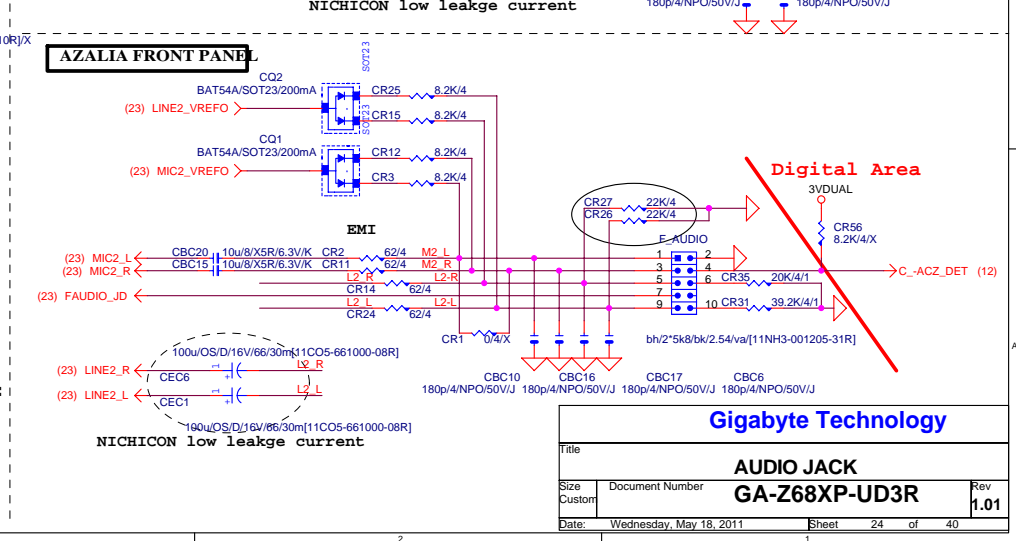
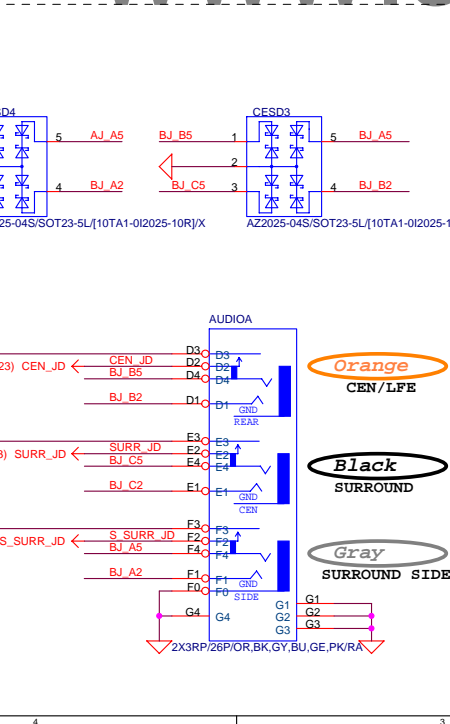
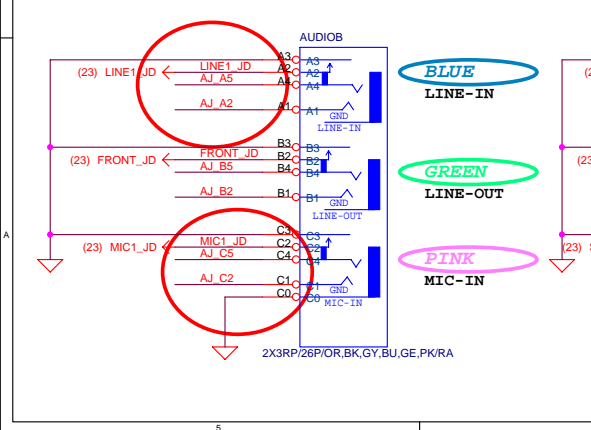
Wednesday, May 18, 2011

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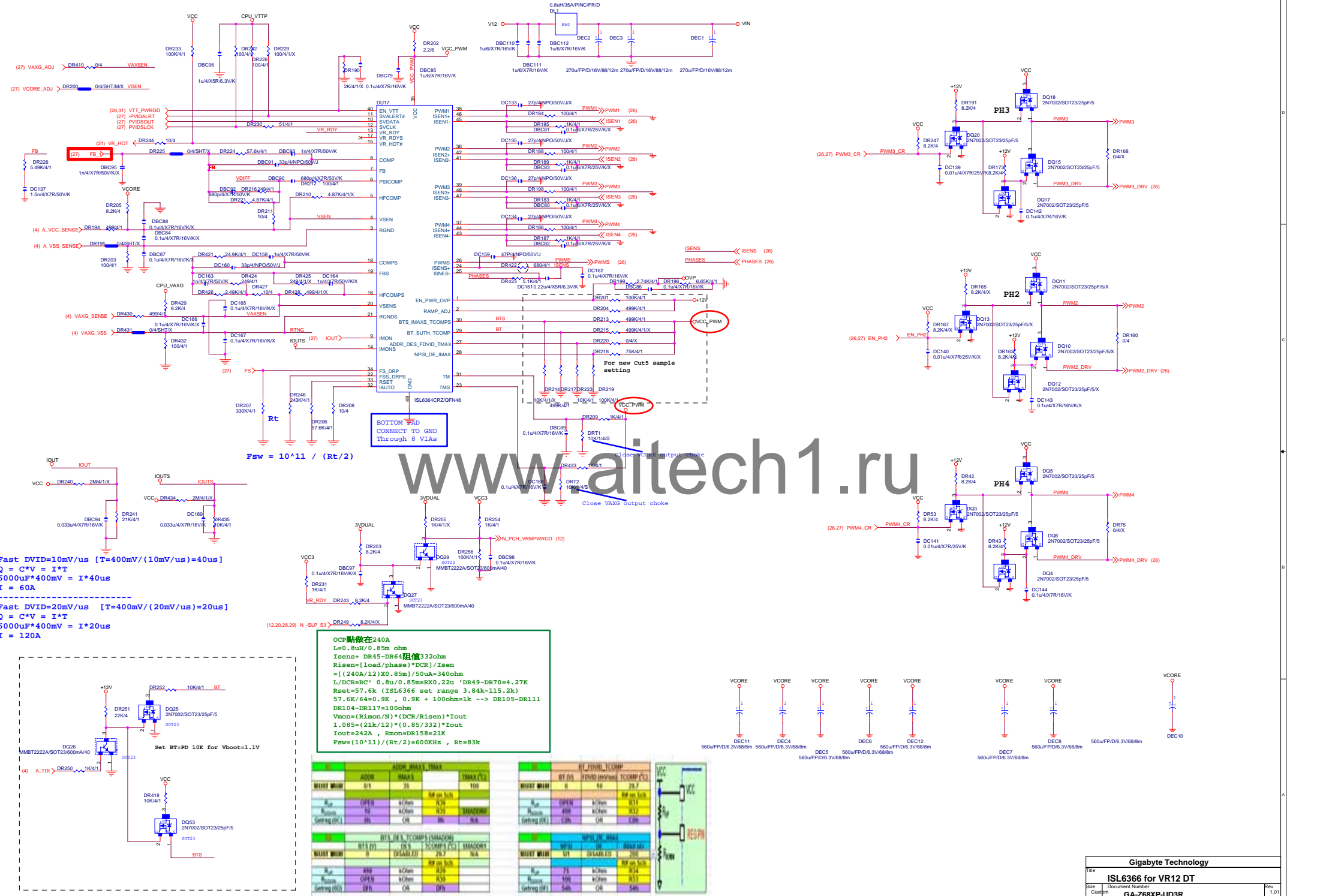
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AUDIO JACK			
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Fast DVID=10mV/us [T=400mV/(10mV/us)=40us]
Q = C*v = I*t
6000uF*400mV = I*40us
I = 60A

Fast DVID=20mV/us [T=400mV/(20mV/us)=20us]
Q = C*v = I*t
6000uF*400mV = I*20us
I = 120A

OC點放在240A
L=0.8uH/0.85m ohm
Isens+ DR45-DR64阻值332ohm
Risen=[load/phase]*DCR/Isen
=[(240A/12)*0.85m]/50uA=340ohm
L/DCR=RC' 0.8u/0.85m=RX0.22u 'DR49-DR70=4.27K
Rset=57.6k (ISL6366 set range 3.84k-115.2k)
57.6K/64=0.9K, 0.9K + 100ohm=1k --> DR105-DR111
DR104-DR117=100ohm
Vmon=(Rmon/N)*(DCR/Risen)*Iout
1.085=(21k/12)*(0.85/332)*Iout
Iout=242A, Rmon=DR158=21K
Fsw=(10*11)/(Rt/2)=600KHz, Rt=83k

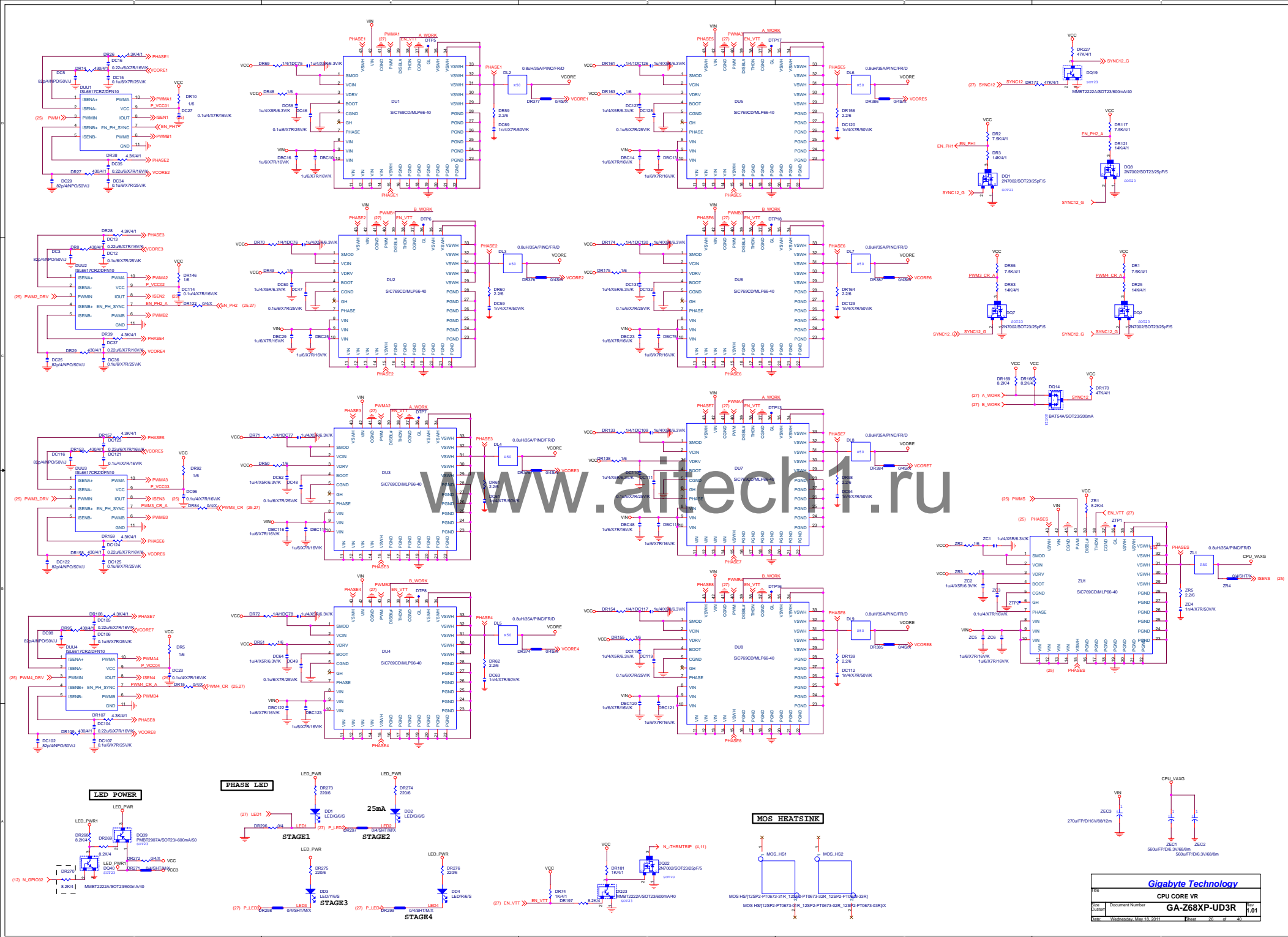
ADJPHASE_TMAX				
MODE	ADJPHASE	TMAX	TMAX (°C)	
MODE	BT	35	100	
R _{DS(on)}	OPEN	10m	10m	10m
R _{DS(on)}	OPEN	10m	10m	10m
Setting (BT)	BT	CH	BT	BT

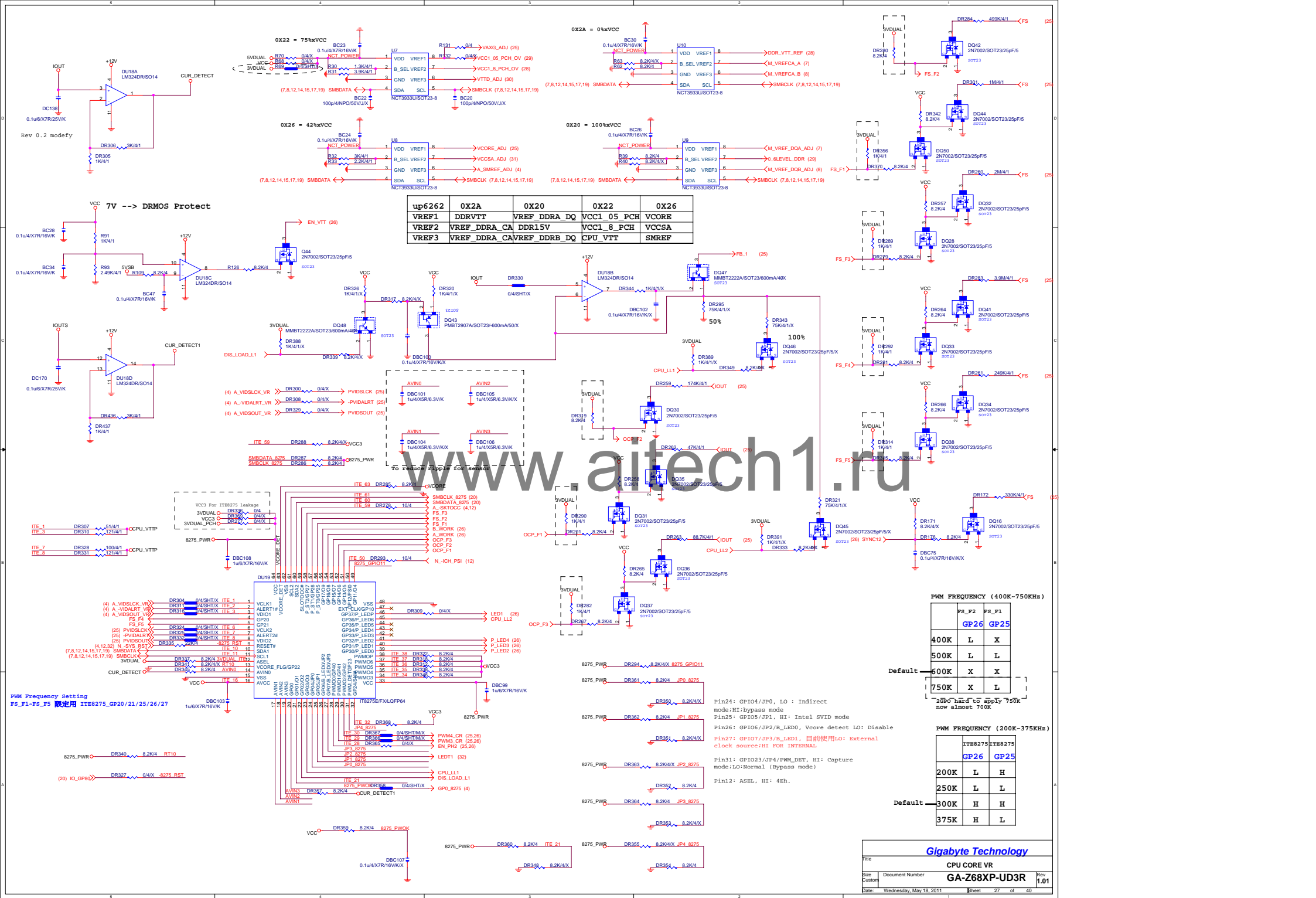
BT_TLVDL_TCOMP				
MODE	BT (V)	TLVDL_TCOMP	TLVDL_TCOMP (°C)	
MODE	BT	10	25.7	
R _{DS(on)}	OPEN	10m	10m	10m
R _{DS(on)}	OPEN	10m	10m	10m
Setting (BT)	BT	CH	BT	BT

BT_DE_TCOMP (MAX/CH)				
MODE	BT (V)	DE_TCOMP	DE_TCOMP (°C)	
MODE	BT	10	25.7	
R _{DS(on)}	OPEN	10m	10m	10m
R _{DS(on)}	OPEN	10m	10m	10m
Setting (BT)	BT	CH	BT	BT

BT_TLVDL_TCOMP				
MODE	BT (V)	TLVDL_TCOMP	TLVDL_TCOMP (°C)	
MODE	BT	10	25.7	
R _{DS(on)}	OPEN	10m	10m	10m
R _{DS(on)}	OPEN	10m	10m	10m
Setting (BT)	BT	CH	BT	BT

BT_DE_TCOMP (MAX/CH)				
MODE	BT (V)	DE_TCOMP	DE_TCOMP (°C)	
MODE	BT	10	25.7	
R _{DS(on)}	OPEN	10m	10m	10m
R _{DS(on)}	OPEN	10m	10m	10m
Setting (BT)	BT	CH	BT	BT



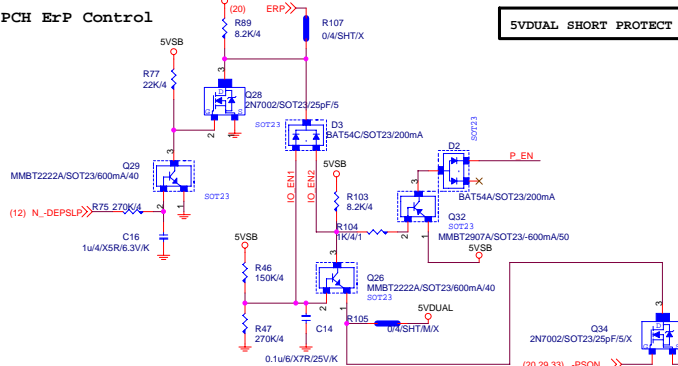
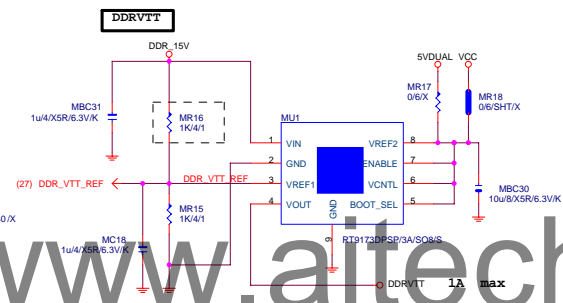
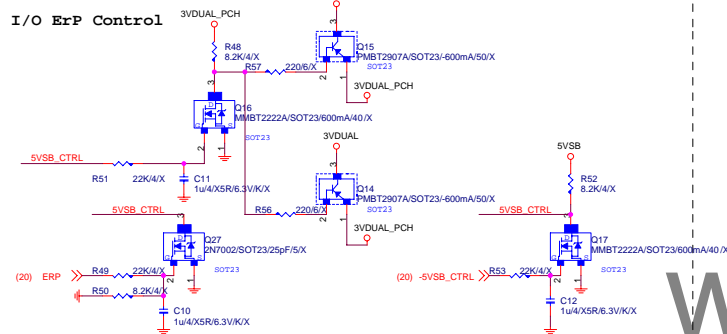
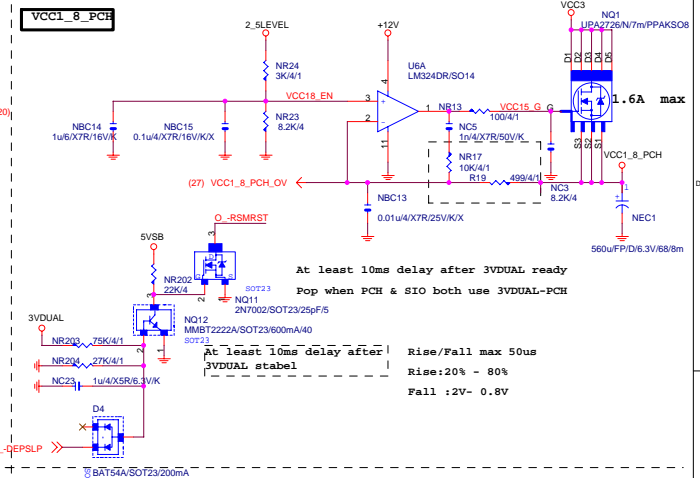
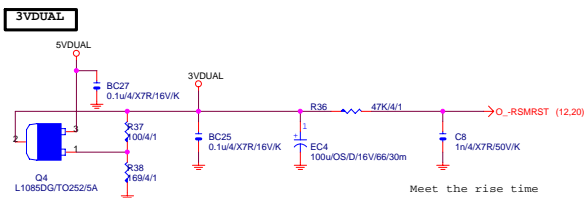
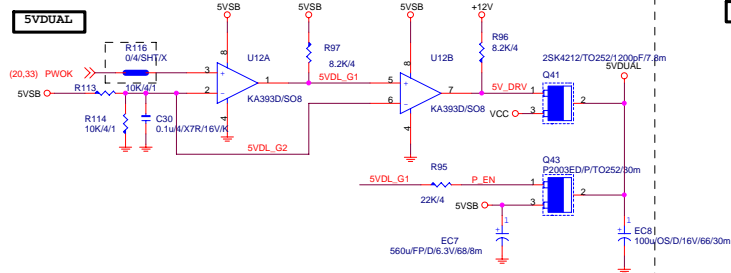


up6262	0X2A	0X20	0X22	0X26
VREF1	DDRVT	VREF_DDRA_DQ	VCC1_05_PCH	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	VCCSA
VREF3	VREF_DDRA_CAVREF_DDRB_DQ		CPU_VTT	SMREF

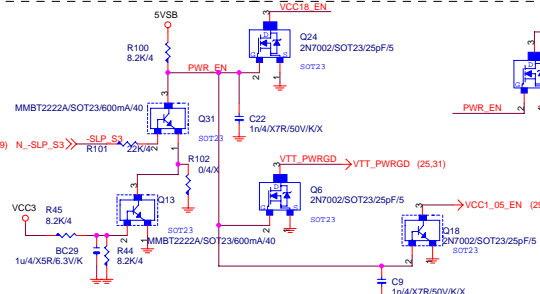
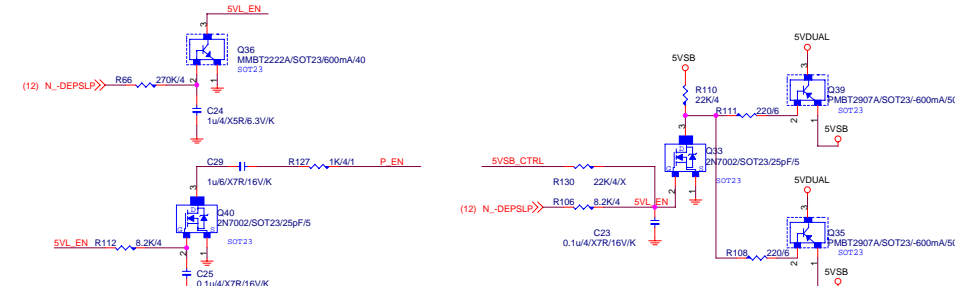
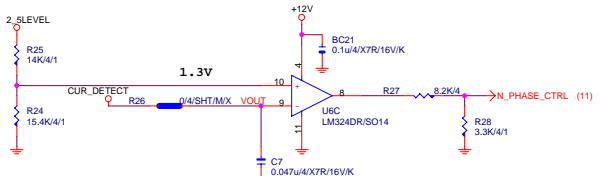
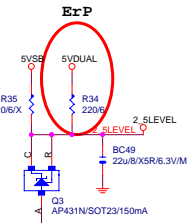
PWM FREQUENCY (400K-750KHz)			
	FS_F2	FS_F1	
	GP26	GP25	
400K	L	X	
500K	L	L	
Default 600K	X	X	
750K	X	L	

2GPO hard to apply 750K now almost 700K

PWM FREQUENCY (200K-375KHz)			
	ITE8275	ITE8275	
	GP26	GP25	
200K	L	H	
250K	L	L	
Default 300K	H	H	
375K	H	L	



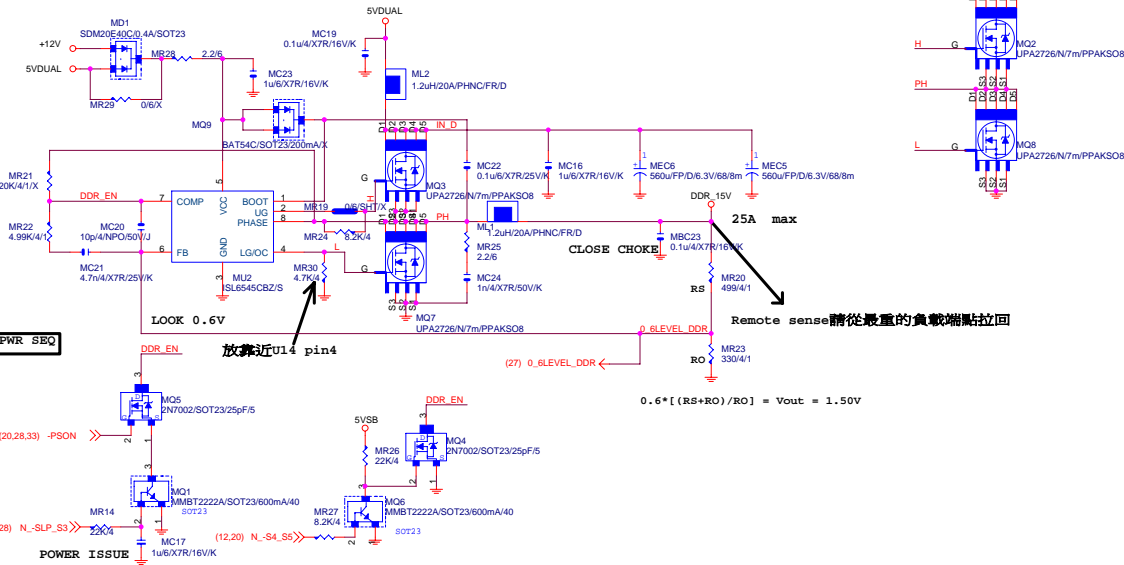
5VDUAL SHORT PROTECT



Gigabyte Technology

DISCRETE POWER			
File	Document Number	GA-Z68XP-UD3R	Rev
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DDR18V



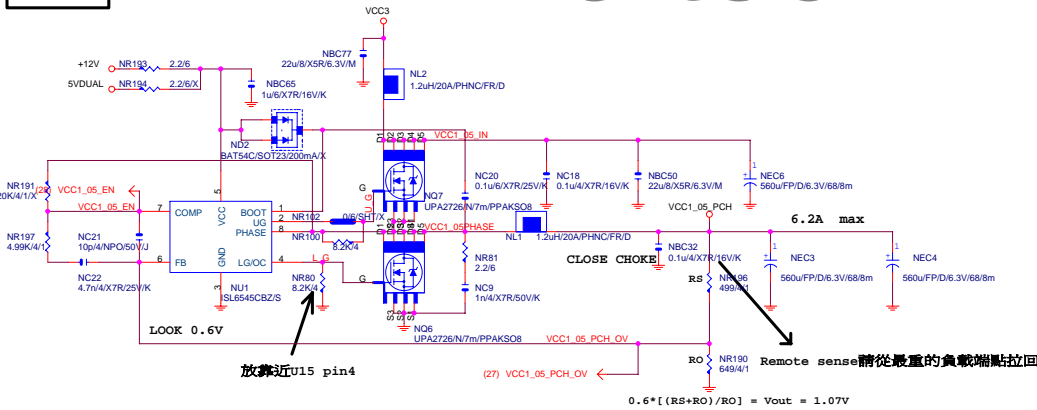
www.aitech1.ru

VCC1_05_PCH

OCP : $I_{peak} = (2 \times I_{ocset} \times R_{ocset}) / R_{dson}$
 $I_{ocset} = 21.5\mu A$, $R_{ocset} = 8.2k$

OCP : $I_{peak} = (2 \times I_{ocset} \times R_{ocset}) / R_{dson}$
 $= (2 \times 21.5\mu A \times 8.2k) / 7m$
 $= 50.37A$

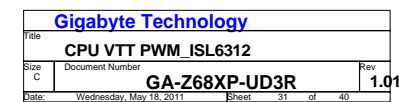
注意：Rocset的阻值要依據Lo side Rdson改變
一般Ipeak設定在50~60A即可



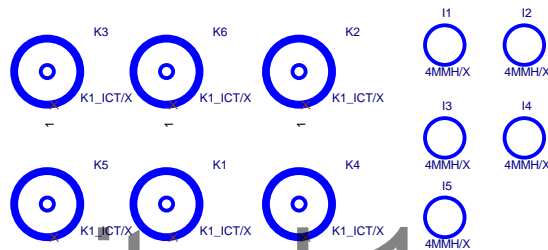
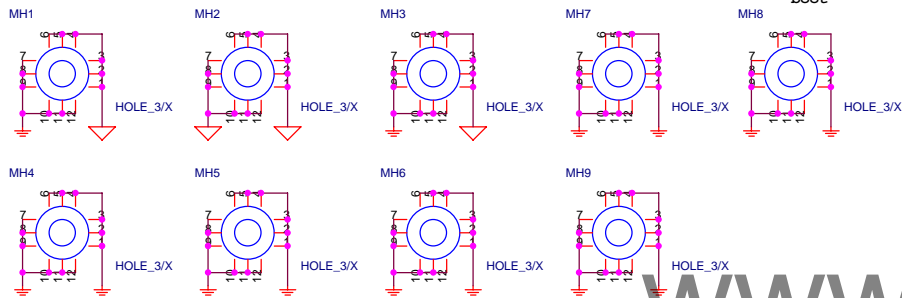
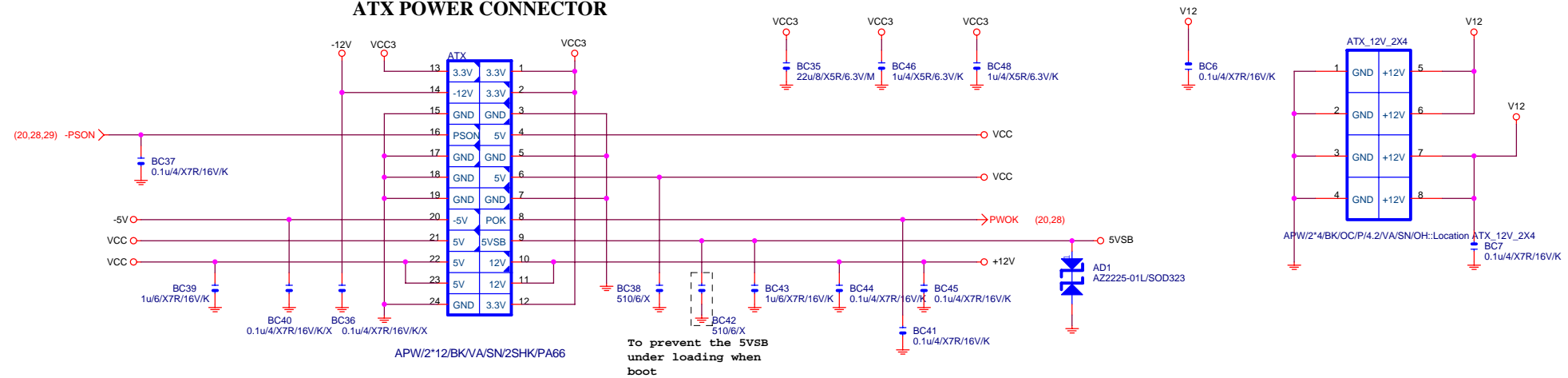
Gigabyte Technology

File	DDR_15V	Rev	1.01
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VCC_SA



ATX POWER CONNECTOR

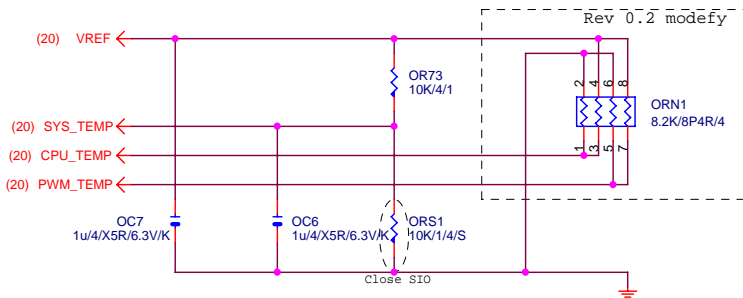


www.aitech1.ru

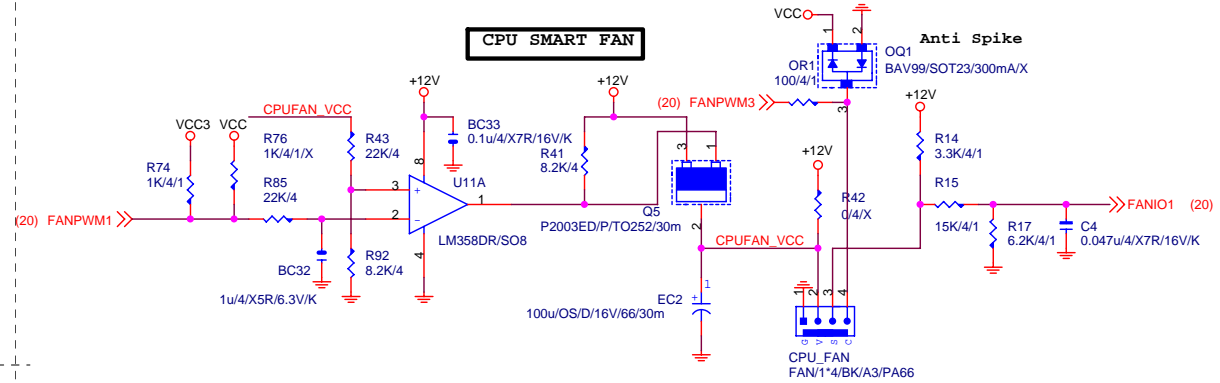
Gigabyte Technology

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ATX POWER CONNECTOR		
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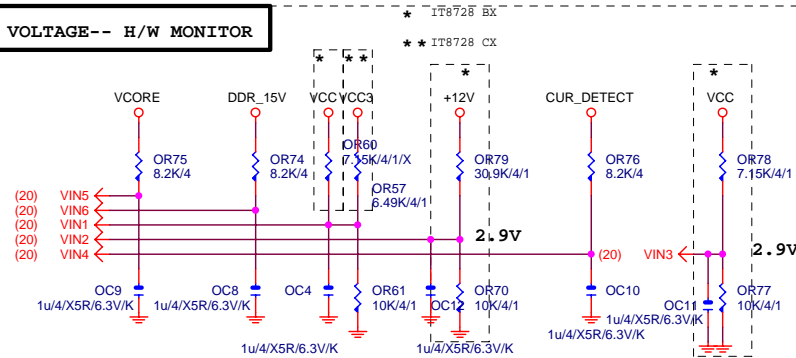
TEMP H/W MONITOR



CPU SMART FAN

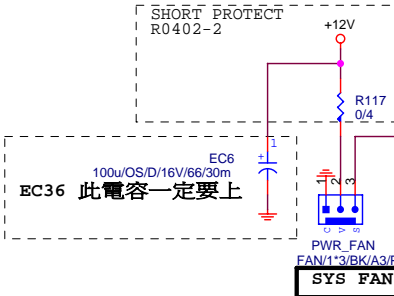
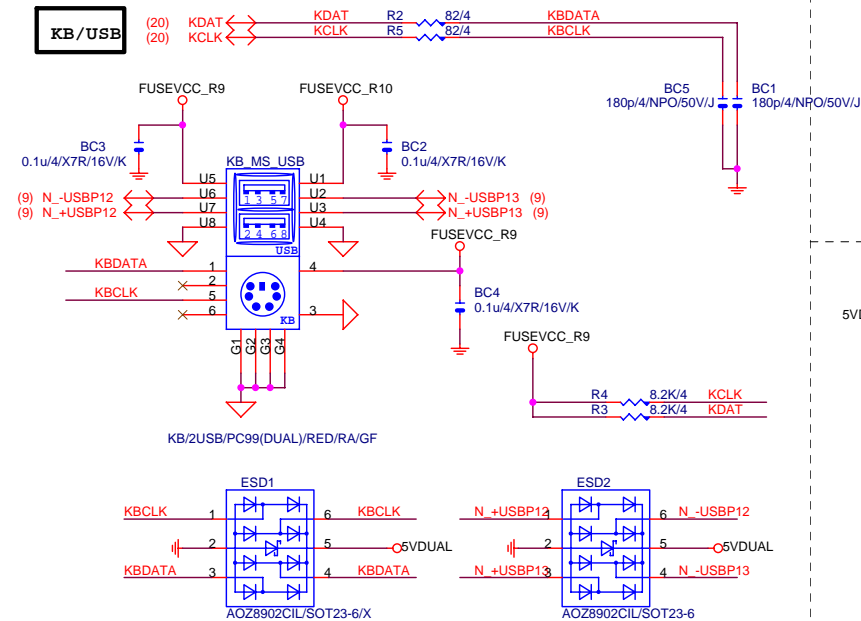


VOLTAGE-- H/W MONITOR

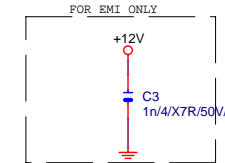
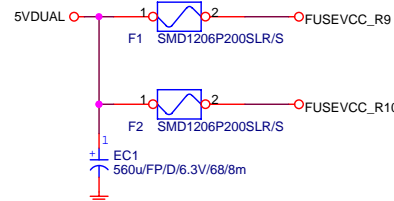
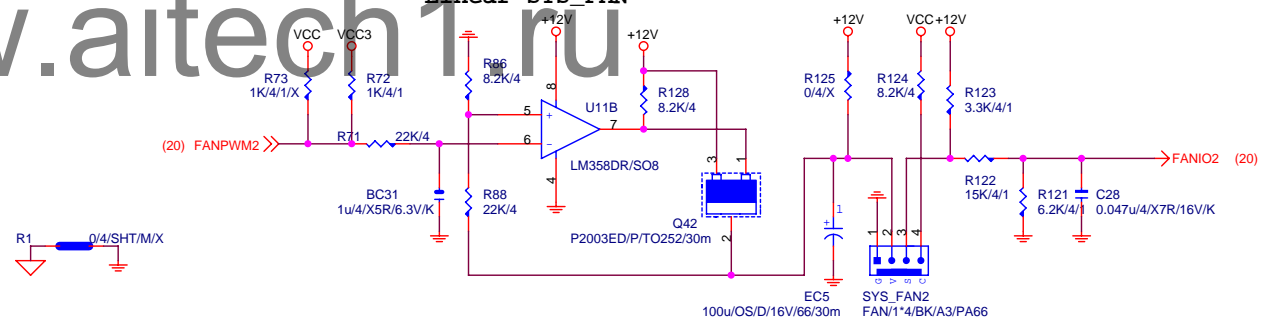


The division voltage of VIN2 & VIN3 must be around 2.9V

KB/USB



Linear SYS_FAN



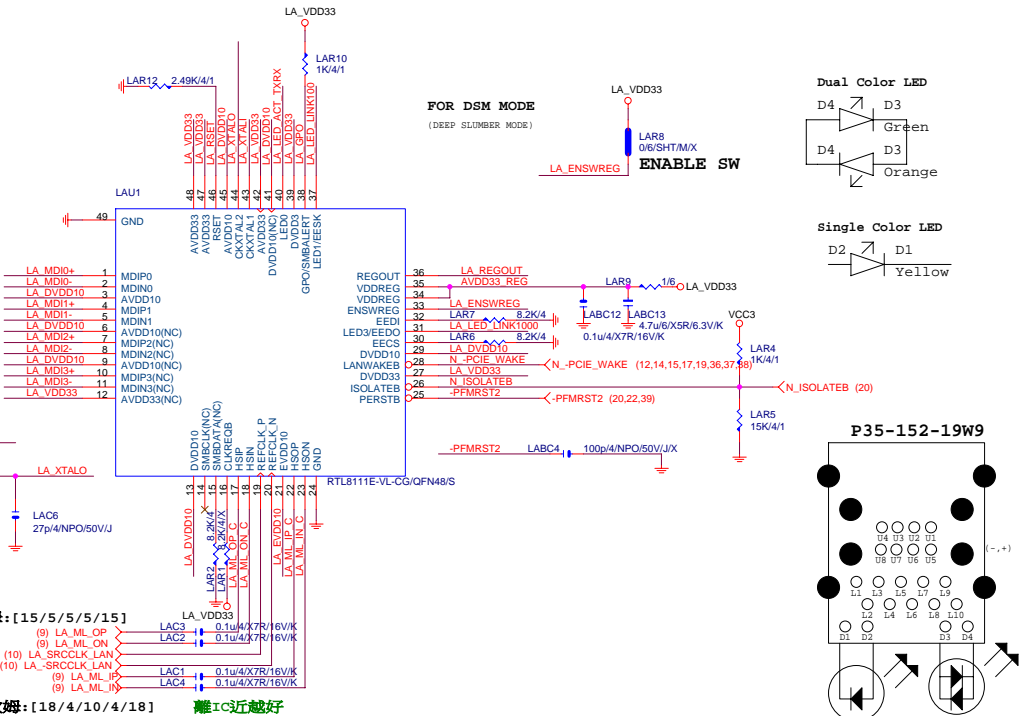
Gigabyte Technology

Title			
HWM,KB/MS, FAN CTRL			
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PCIE-1G LAN

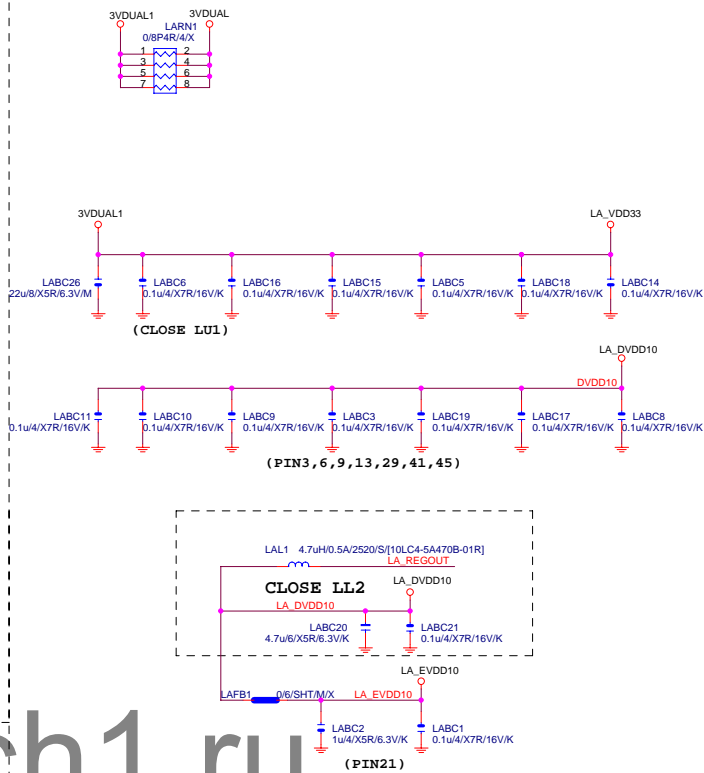
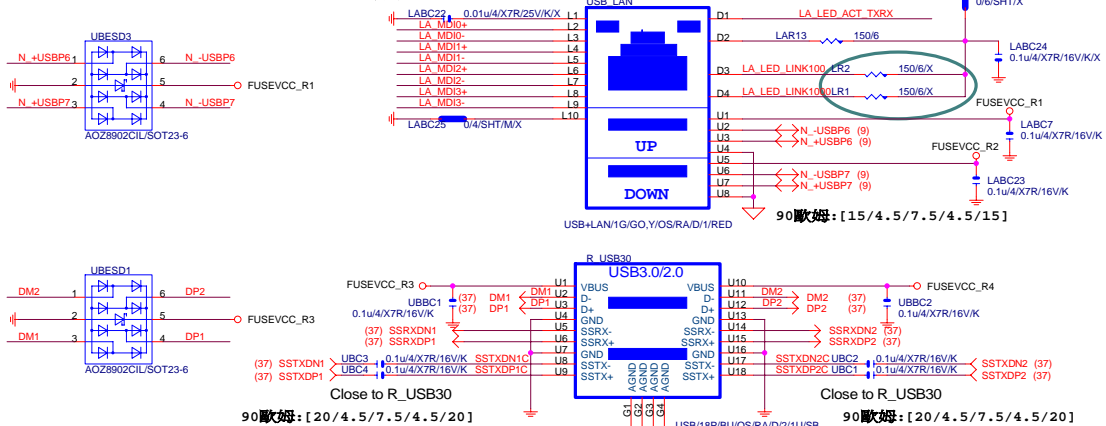
Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

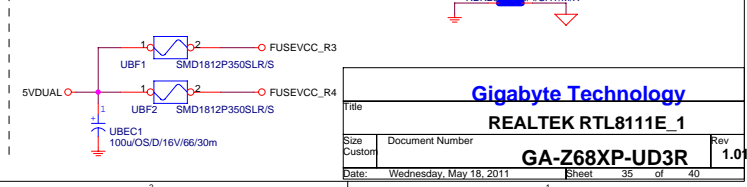


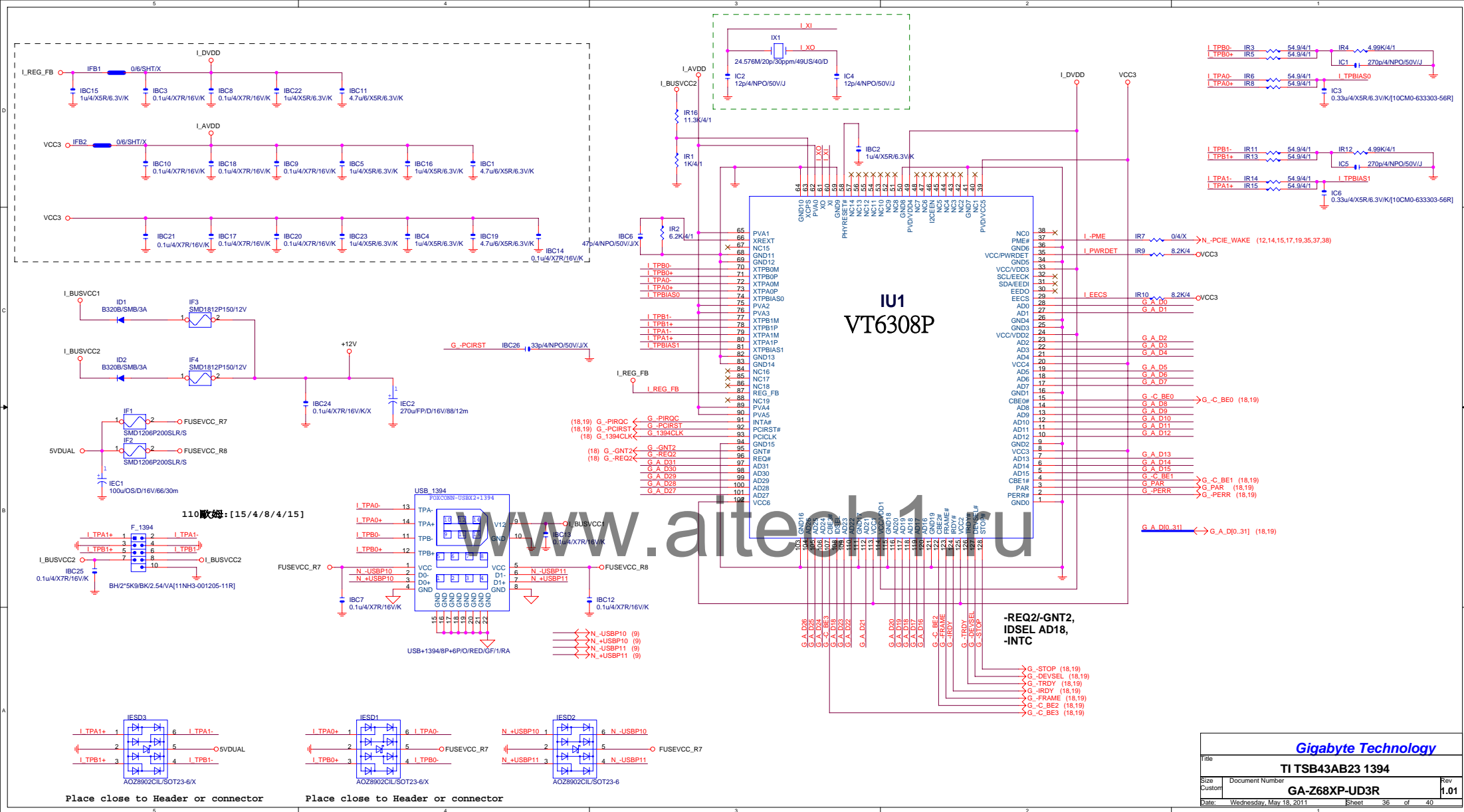
USB30_LAN CONNECTOR

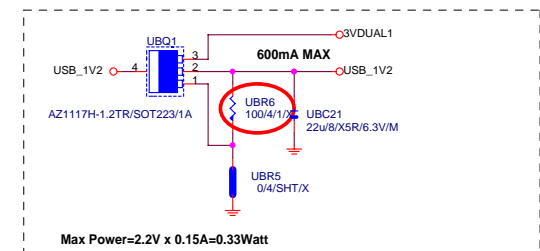
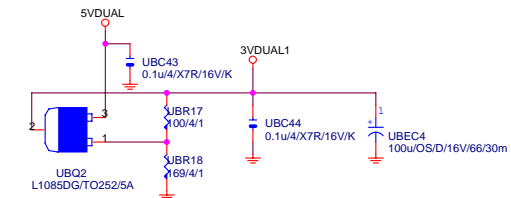
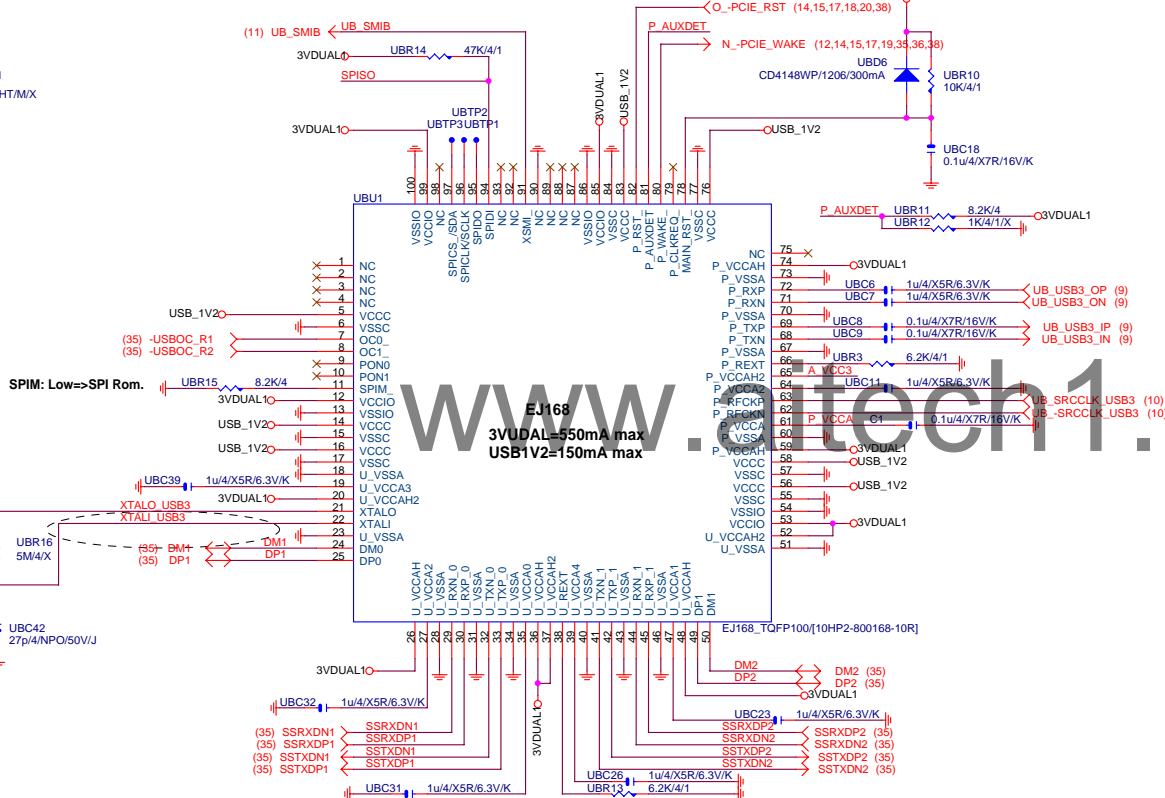
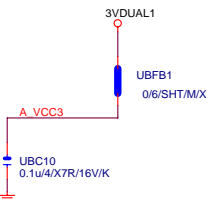
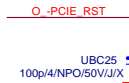
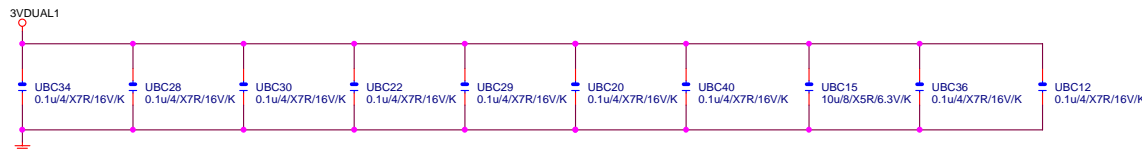
100 欧姆: [20/4/8/4/20]



Close to connector







Max Power=2.2V x 0.15A=0.33Watt

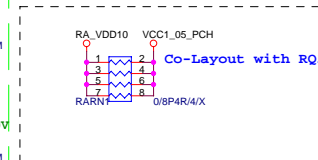
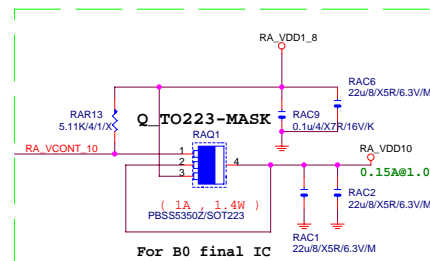
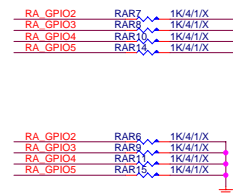
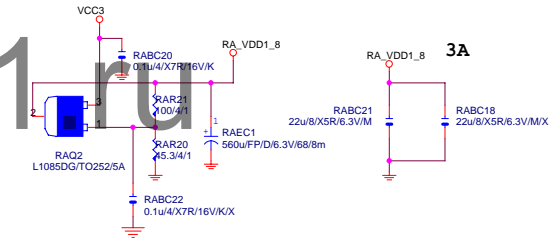
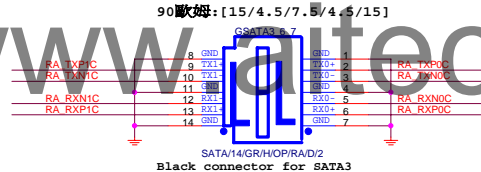
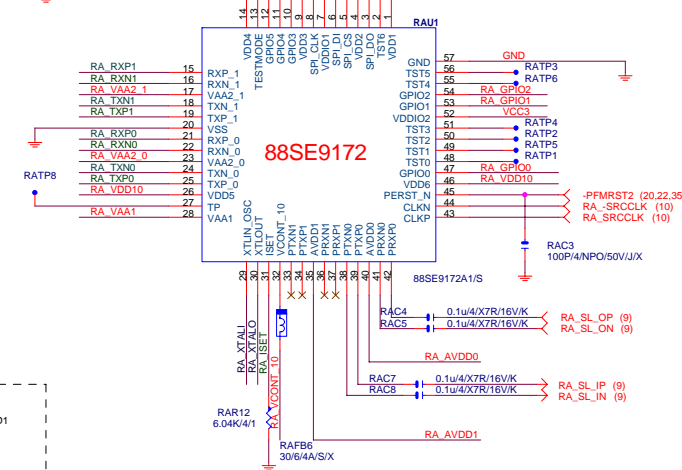
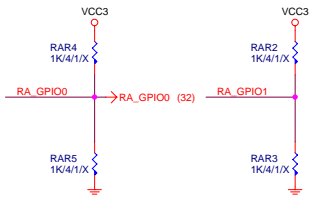
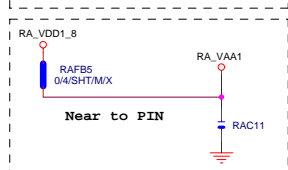
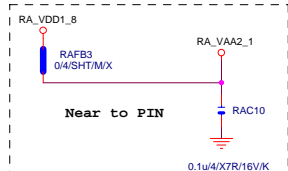
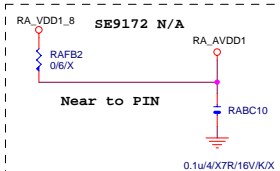
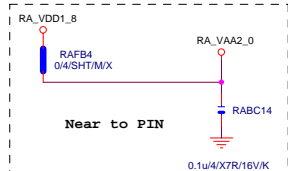
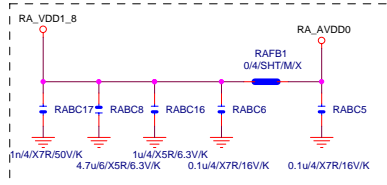
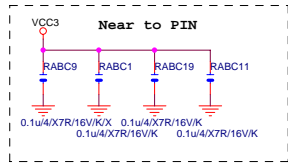
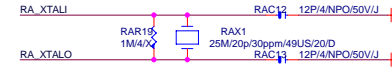
AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]

L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]

USB3.0 --> 5GHz

BANDWITH=5GHz*(8b/10b)=4Gb/s=500MB/s

GIGABYTE			
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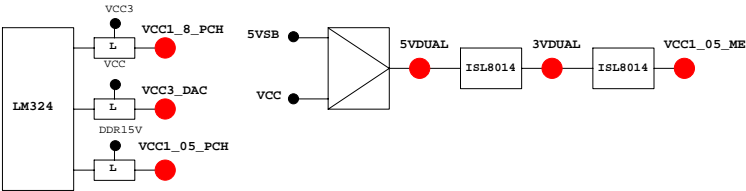


PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

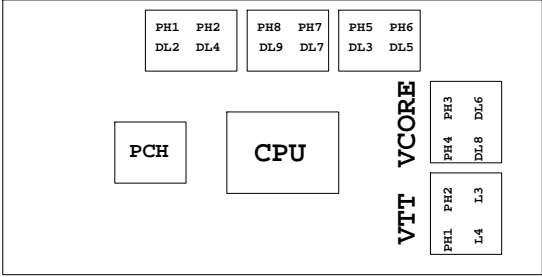
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SFI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AED#/GP86/SMBD_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBD_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

散熱模組料號：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

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